32nd IEEE COMPOUND SEMICONDUCTOR IC (CSIC) SYMPOSIUM

Program

Presenting:

CSICS: Back in the Bay

Oct 3rd – Oct 6th, 2010
Portola Hotel & Spa

Monterey, California, USA

CO- SPONSORED BY
The IEEE Electron Devices Society,
The IEEE Solid-State Circuits Society, and
The IEEE Microwave Theory and Techniques Society.

SYMPOSIUM

Saturday, October 2nd, 2010
REGISTRATION (Short Course & Primer Course Only)

Sunday, October 3rd, 2010
REGISTRATION (Short Course & Primer Course Only)
Short Course Continental Breakfast
SHORT COURSE 1: High Performance Linear Transceiver MMIC Design
SHORT COURSE 2: High-Speed and mm-Wave Digital-Rich Transceiver Design
Short Course Lunch
REGISTRATION for Symposium (and Primer Course until 4:00pm)
PRIMER COURSE: Basics of Compound Semiconductor ICs
CSIC Symposium Opening Reception

Monday, October 4th, 2010
REGISTRATION
Continental Breakfast
SYMPOSIUM OPENING
SESSION A: Plenary Session
SESSION B: Handset and Basestation Front-Ends
SESSION C: GaN HEMT Modeling
SESSION D: High Speed Digital Circuits
PANEL SESSION 1: X-Parameters and Measurement-Based Behavioral Models: Real Models or Just Marketing?
Exhibition Opening Reception

Tuesday, October 5th, 2010
REGISTRATION
Technology Exhibition
Continental Breakfast
SESSION E: Ultra Low Noise Receivers for Radio Astronomy
SESSION F: III-V Advanced IC Technology
SESSION G: Digital and Optoelectronic Systems
SESSION H: III-V/Silicon Heterogeneous Integration
Exhibition Luncheon
PANEL SESSION 2: Ultra High-Speed Test and Measurement: Can instrument vendors keep up and can IC developers afford it?
PANEL SESSION 3: Changing MMIC EDA Design Flows & Tools: Lessons Learned and Future Directions.
SESSION I: High Speed Digital and mm-Wave CMOS
Symposium Theme Party

Wednesday, October 6th, 2010
REGISTRATION
Continental Breakfast
SESSION J: Power and Switching GaN Devices
SESSION K: mm-Wave Oscillators and Phase Shifters
PANEL SESSION 4: Foundry Capabilities and Services for Advanced III-V Processes
SESSION L: Power Amplifiers for Microwave and MMW Applications
SESSION M: GaN and GaAs HFETs
SESSION N: mm-Wave to THz Mixing Technologies
SESSION O: Late News Papers
SESSION P: Late News Papers
Close of Symposium

AT A GLANCE

Saturday, October 2nd, 2010

4:00 p.m. – 6:00 p.m.	De Anza Foyer

Sunday, October 3rd, 2010

7:00 a.m. – 8:00 a.m.	De Anza Foyer
7:00 a.m. – 8:00 a.m.	**De Anza III**
8:00 a.m. – 5:00 p.m.	Bonsai I
8:00 a.m. – 5:00 p.m.	Bonsai II
12:15 p.m. – 1:45 p.m.	**De Anza III**
3:00 p.m. – 8:00 p.m.	De Anza Foyer
4:00 p.m. – 7:00 p.m.	Bonsai III
6:00 p.m. – 8:00 p.m.	**Lower Atrium**

Monday, October 4th, 2010

7:00 a.m. – 5:00 p.m.	De Anza Foyer
7:00 a.m. – 8:30 a.m.	**De Anza Foyer/Lower Atrium**
8:30 a.m. – 9:00 a.m.	De Anza III
9:00 a.m. – 11:00 a.m.	De Anza III
1:30 p.m. – 3:20 p.m.	De Anza III
1:30 p.m. – 3:10 p.m.	De Anza II
3:30 p.m. – 4:50 p.m.	De Anza III
3:30 p.m. – 5:00 p.m.	De Anza II
5:30 p.m. – 8:00 p.m.	**De Anza I**

Tuesday, October 5th, 2010

7:00 a.m. – 5:00 p.m.	De Anza Foyer
8:00 a.m. – 5:00 p.m.	De Anza I
7:00 a.m. – 8:30 a.m.	**De Anza 1**
8:30 a.m. – 10:10 a.m.	De Anza III
8:30 a.m. – 10:00 a.m.	De Anza II
10:30 a.m. – 12:00 p.m.	De Anza III
10:30 a.m. – 12:20 p.m.	De Anza II
12:00 p.m. –1:30 p.m.	**De Anza I**
1:30 p.m. – 3:00 p.m.	De Anza II
3:30 p.m. – 5:00 p.m.	De Anza III
3:30 p.m. – 5:15 p.m.	De Anza II
6:00 p.m. – 10:00 p.m.	**Memory Gardens**

Wednesday, October 6th, 2010

7:00 a.m. – 2:00 p.m.	De Anza Foyer
7:00 a.m. – 8:30 a.m.	**De Anza Foyer/Lower Atrium**
8:30 a.m. – 10:00 a.m.	De Anza III
8:30 a.m. – 9:50 a.m.	De Anza II
10:30 a.m. – 12:00 p.m.	De Anza III
10:30 a.m. – 12:00 p.m.	De Anza II
1:30 p.m. – 3:20 p.m.	De Anza III
1:30 p.m. – 2:30 p.m.	De Anza II
3:30 p.m. – 5:10 p.m.	De Anza III
3:30 p.m. – 5:10 p.m.	De Anza II
5:10 p.m.	

Visit us at: http://www.csics.org

CHAIR'S MESSAGE

On behalf of the organizing committee and the IEEE Electron Devices Society, the Microwave Theory and Techniques Society, and the Solid-State Circuits Society, we invite you to be a part of the 2010 IEEE Compound Semiconductor IC Symposium (CSICS). This year's symposium will be held October 3rd – October 6th in Monterey, CA.

This will be the 32nd year that the IEEE CSICS (originally GaAs IC Symposium) has been held. We have chosen to locate in what has become the home away from home for CSICS, namely Monterey. This will be the seventh time we have located in Monterey.

If we go back in time to 1979, it is doubtful that any but the most optimistic persons imagined that 30 years later GaAs would be a mainstream commercialized semiconductor. What started as an exotic, high-speed semiconductor for digital applications morphed into a major player in analog defense electronics and has now become a fully commercialized multi-billion dollar industry. Along the way, government and corporate sponsorship enabled substantial research on GaAs and related III-V compounds that led to advances in materials growth, device characterization, device physics and higher levels of integration. As GaAs technology matured, other III-V material systems were explored in depth, as well as some advanced device structures. As a result, the Symposium changed its name to IEEE Compound Semiconductor IC Symposium (CSICS) in 2004 to reflect the evolution of the III-V industry and the interests of its participants.

The CSIC Symposium has always been the top international forum on developments in integrated circuits using compound semiconductors such as GaAs, InP, GaN, SiGe and other III-V and II-VI materials. It covers all aspects of the technology, from material issues and device fabrication, through IC design and testing, high volume manufacturing, and system applications.

There are several social events that allow our attendees to interact in a relaxed setting. These include the Sunday Evening Opening Reception, the Monday evening Technology Exhibition Opening Reception, the Tuesday Technology Exhibition Luncheon, and the Tuesday evening Theme Party. This year's Theme Party provides a laid back California environment and should be enjoyable. We also offer daily breakfast and AM/PM coffee breaks Monday through Wednesday.

The IEEE CSICS will offer two short courses this year. The first will be "High Performance Linear Transceiver MMIC Design" and the second will be "High-Speed and mm-Wave Digital-Rich Transceiver Design". Both of these will be taught on Sunday Oct. 3rd, 2010. The first course covers transceiver design and includes some real world examples. The second course will explore the world of digital-rich high frequency fiber optics and mm-Wave transceivers. Both courses utilize a blend of experts from industry and leading universities. In addition, we offer our "Primer Course" on the basics of semiconductor ICs which is an excellent tutorial presented within the context of our Symposium technical program. The Primer Course is also offered on Sunday Oct.3rd, 2010.

We hope to see you this year when we go back to the bay!

David Halchin, Chair

2010 IEEE CSICS

CORPORATE BENEFACTORS

This year, we are pleased to continue with the IEEE Compound Semiconductor IC Symposium Corporate Benefactors Program. This program allows companies interested in compound semiconductors to show their support of the Symposium by making contributions towards the cost of some of our social events.

These additional resources enable the Symposium to increase the quality of our event, as well as allowing companies an opportunity for some tasteful promotional activities. To discuss any of the benefactor opportunities in more depth, please contact:

Dave Halchin
Tel: +1-336-678-8123
E-mail: dhalchin@rfmd.com

As of this printing, the Corporate Benefactors for the 2010 Compound Semiconductor IC Symposium are as follows.

Gold Level Benefactors :

RF Micro Devices, Inc.

TriQuint Semiconductor

Silver Level Benefactors:

OMMIC
AWR Corporation

The Symposium Web Site www.csics.org has become a critical tool for the dissemination of information to prospective attendees, committee members and sponsors of the Symposium. Every year, the web site must be updated and maintained to effectively serve this purpose. We would like to acknowledge the following benefactor for providing the Symposium web site support for the 2010 CSIC Symposium:

Comments regarding the web site or any publicity materials should be directed to the Publicity Chair, Charles Campbell (Charles.campbell@tqs.com). Links to our corporate benefactors appear on our symposium website.

GENERAL INFORMATION

IEEE 32nd CSIC Symposium
Oct 3rd - Oct 6th, 2010
Portola Plaza and Spa
Monterey, CA

REGISTRATION

	Advance (Received by Sept. 10th)	Regular (After Sept. 10th or on site)
Symposium Registration		
IEEE Member	$590	$640
Non-IEEE	$695	$760
IEEE Life-Member	$290	$320
Student	$290	$350
Special One-day IEEE Member[1]	$300	$350
Special One Day Non-IEEE[1]	$355	$415
Short/Primer Course		
Short Course	$400	$400
Short Course Student	$200	$200
Primer Course	$175	$175
Primer Course Student	$100	$100
Additional Items		
Guest Opening Reception Ticket	$50	$50
Guest Theme Party Ticket	$75	$130
Adtl. Technical Digest	$110	$110
Adtl. Digest USB	$100	$100
Adtl. Short Course CD ROM	$100	$100
Adtl. Primer Course Notes	$50	$50

All fees are denominated in US$
Full Registration Includes: Technical Digest, USB Digest, Opening Reception, Theme Party, all technical sessions, panels, exhibits, Exhibition Opening Reception and Exhibition Lunch.
Short Course Registration Includes: Short Course Notes and CD-ROM , continental breakfast and Short Course Lunch
[1]Special One-day Registration Includes: CD-ROM only (no social functions)
Primer Course Registration includes: Primer Course Notes Only

For **ADVANCE REGISTRATION,** click on the Symposium Registration link on the Symposium website (www.csics.org). You may register either through the website or complete the enclosed Advance Registration Form with your remittance of the appropriate fee (check or credit card) **By September 10th, 2010**. Prices will increase after the September 10th deadline.

Mail or Fax Completed Advance Registration Form to:

IEEE/MCM: Lukrecija Lelong, CSICS Registrar,
445 Hoes Lane, Piscataway, NJ, 08854 USA
Tel: +1-732-562-5441
Toll Free (US or Canada) +1-800-810-4333
FAX : +1-732-465-6447
Email: csics10reg@ieee.org

The remittance is payable by checks in U.S. dollars only, by personal/company check drawn on a U.S. bank, U.S. currency traveler's checks, or international money order. Checks must be made payable to "IEEE/2010 CSICS" and must be encoded with the bank number, account number, and check number. Credit cards and wire transfers may also be used. Bank drafts from non-U.S. banks and foreign currency are unacceptable and will be returned.

When you register for the Conference, the contact information you provide (including your name, address, phone, and email address) may be shared with CSICS and vendor exhibitors.

We urge you to pre-register to reduce your costs and to simplify your check-in at the Symposium. Your Technical Digest and registration materials will be ready for you at the Advance Registration Desk.

Registration Center:

The Symposium Registration Center is located in the De Anza Foyer on Saturday through Wednesday. The operating hours will be as follows:

Short & Primer Course Registration only

Saturday, October 2nd	4:00 p.m. – 6:00 p.m.
Sunday, October 3rd	7:00 a.m. – 8:30 a.m.
Sunday, October 3rd	3:00 p.m. – 4:00 p.m. (Primer)

Symposium Registration

Saturday, October 2nd	4:00 p.m. – 6:00 p.m.
Sunday, October 3rd	3:00 p.m. – 8:00 p.m.
Monday, October 4th	7:00 a.m. – 5:00 p.m.
Tuesday, October 5th	7:00 a.m. – 5:00 p.m.
Wednesday, October 6th	7:00 a.m. – 2:00 p.m.

Refund Policy:

All requests for refund/cancellation must be received in writing by September 10th, 2010. No refunds can be provided after this date. Cancellations will incur a $25 administration fee. Please submit cancellation requests via email to csics10reg@ieee.org

ACCOMMODATIONS

Hotel Reservations:

A block of rooms has been reserved at special discounted rates for Symposium participants at our headquarters hotel, the Portola Hotel & Spa at Monterey Bay. Located in the heart of Monterey, the Portola Hotel is adjacent to the Monterey Conference Center. The hotel overlooks the scenic Fisherman's Wharf and the Monterey Bay. It is only four miles from the Monterey Peninsula Airport. Set against the picturesque backdrop of Monterey Bay, Fisherman's Wharf and downtown Monterey, the Portola Hotel is within walking distance to the world-class Monterey Bay Aquarium, pristine beaches, Monterey Bay harbor and hundreds of dining and entertainment options.

The hotel guest rooms offer cable TV, complimentary internet access, telephones with voice messaging and a mini-bar. Rooms are available for non-smokers and with wheelchair access. They also feature room service, restaurants, cafes, cocktail lounges with entertainment, sports bars, outdoor pool and spa, health club, and many fine shops.

Hotel Address and Phone Numbers:

Portola Hotel & Spa at Monterey Bay
2 Portola Plaza
Monterey, CA 93940
Phone: 831-649-4511
Fax: 831-649-4115
Guest Fax: 831-372-0620

We ask you to please support your Symposium and more fully enjoy all the activities by staying at our official headquarters hotel. The Symposium relies on attendees staying at the Portola Hotel to reduce the costs charged for the use of meeting rooms. Room reservations should be made as soon as possible, and no later than September 2, 2010, 5pm Pacific Time. Rooms are available at the special Symposium group rate of $185 single or double per night. These rates do not include room taxes, currently 10.065 percent plus $1 Monterey County Tourism Assessment. A limited number of rooms have been set aside for the use of bonafide U.S. government employees at the prevailing government rate.

To make a reservation please call the hotel direct at 831-649-4511 and ask for Reservations. Be certain to request the Special Group Rate for the IEEE CSIC Symposium. Other regional hotels will not be aware of the discounted rate for the Symposium.

It is strongly recommended that you call the hotel direct thereby obtaining an immediate confirmation. If you choose to mail or fax your request, be sure to follow up on it. After the September 2, 2010 deadline, rooms will be on a space available basis at possibly higher rates. Check-in time is 3 p.m. or later; check-out time is 12 noon. If necessary, you may cancel your reservation at the Portola Hotel up to 6:00 p.m. on the day of your scheduled arrival.

TRANSPORTATION

Travel Arrangements:

Special Airfares:

Travel arrangements using the IEEE negotiated air carriers or the carriers of your choice can be made through World Travel, Inc by calling between the hours of 8:00 a.m. and 5:30 p.m. EST. Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (+1 800 879 4333); and outside of the US and Canada, call +1 717 556 1100. Or, you may visit their on-line travel service web site at http://www.ieee.org/travel. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere. Or you can e-mail your request to ieee@worldtravelinc.com.

IEEE corporate car rental discounts are also available to all attendees of the symposium. Discount codes below entitle attendees to receive special rates that have also been negotiated with Avis A606000, Budget X520000, Hertz 61368, and Enterprise NA24IE1.

Airport Transportation:

The Monterey Peninsula Airport, serving one of the world's favorite destinations for both business and pleasure, offers commercial service with convenient connecting flights to and from anywhere in the world. Or you can fly into the area's major airports, San Jose, San Francisco, and Oakland Airport and take the scenic drive to Monterey.

Approximate Driving Times:
Monterey Peninsula Airport - 10 Minutes
San Jose Airport - 1.5 Hours
San Francisco Airport - 2.0 Hours
Oakland Airport - 2.0 Hours

Driving Directions:

From Monterey Peninsula Airport/Highway 68 from Salinas:
Take the Monterey Fisherman's Wharf exit, at first light turn right onto Aguajito, turn left onto Del Monte, at third light get into left lane and the Portola Hotel will be to your right.

From North on Highway 1:

Take the Del Monte/Pacific Grove exit, at seventh light, get into the left lane, and drive until you get to the Portola Hotel which will be to your right.

From South/Carmel on Highway 1:

Take the Aguajito exit, turn left at the first light (going under the freeway), follow Aguajito to Del Monte, turn left onto Del Monte, at third light get into left lane and the Portola Hotel will be on your right.

ADDITIONAL INFORMATION

Distribution of Relevant Information:

The CSIC Symposium will provide an officially designated area near the registration desk to serve as the proper display area for those in need of space to disseminate free material relevant to the CSIC industry. Printed material of any form will not be allowed to be indiscriminately proliferated in the registration area, hallways, lobbies, or other gathering areas, in proximity to the Symposium, technical sessions, evening social activities, panel sessions, or the exhibition. A message board will be placed near the registration desk for people trying to reconnect onsite, to post CFPs and job opportunities.

No Photographic and/or Recording Equipment:

No photographic or recording equipment will be permitted at any time during the technical sessions of the IEEE CSIC Symposium.

Breakfast and Lunch Locations:

Breakfasts:

The location of breakfasts will be as follows:

Short Course Registrants (only) –
Sunday, October 3rd: De Anza III

Symposium Registrants –
Monday, October 4th: De Anza Foyer/ Lower Atrium
Tuesday, October 5th: De Anza I
Wednesday, October 6th: De Anza Foyer/ Lower Atrium

Lunches:

The location of lunches will be as follows:

Short Course Registrants (only) –
Sunday, October 3rd: De Anza III

Symposium Registrants –
Tuesday, October 5th: De Anza I

Coffee Breaks:

The location of coffee breaks will be as follows:

Short Course Registrants (only) –
Sunday, October 3rd: Bonsai I & II

Symposium Registrants –
Monday, October 4th: De Anza Foyer/Lower Atrium
Tuesday, October 5th: De Anza I
Wednesday, October 6th: De Anza Foyer/Lower Atrium

Symposium Social Events:

SYMPOSIUM OPENING RECEPTION

We welcome you to Monterey on Sunday evening, October 3rd from 6:00 p.m. to 8:00 p.m. in the Lower Atrium of the Portola Hotel. Come and meet up with your old friends and make new acquaintances over cheese and wine, beer, or soft drinks. One free admission is included with your registration including two drink tickets, and extra reception tickets may be purchased at registration for $50.

EXHIBITION OPENING RECEPTION

Our exhibitors are hosting a reception to mark the exhibition opening on Monday, October 4th from 5:30 p.m. to 8:00 p.m in De Anza I. Every Symposium participant is invited to enjoy the hors d'oeuvres and schmooze and cruise the exhibits.

EXHIBITION LUNCH

On Tuesday October 5th at noon the Exhibition Luncheon will be hosted in De Anza I. The lunch is free to all Symposium participants, so come along, visit with the exhibitors, ask questions, make deals and find out what is going on in our industry.

SYMPOSIUM PARTY

Join us for the Symposium Theme Party on Tuesday, October 5th, from 6:00pm to 10:00pm for an evening of jazz with the Cory Wright Quartet in the Memory Gardens adjacent to the Portola Hotel. Our Monterey Fisherman's Warf menu will feature a delightful selection of fresh crudités followed by Paella Valencia and Harris Ranch Prime Rib.

This fascinating atmosphere and the good food and refreshments will provide an excellent time to meet with colleagues old and new. One free admission to the Symposium Party is included with each full registration, and extra tickets can be purchased on site for $115.

Monterey Attractions:

Among the many features Monterey itself has to offer is historic Cannery Row, a popular visitor area offering a multitude of unique galleries, shops, wine tasting rooms, and restaurants. Fisherman's Wharf, once the center of Monterey's fishing industry, also offers seafood restaurants, fish markets, and specialty shops. Sight-seeing and whale-watching charter and tour companies operate off the wharf daily. Within driving distance of Monterey are numerous wineries offering tours, as well as opportunities for scenic hiking, biking, water sports, golf, and even rock climbing.

Monterey Weather:

There is a significant variance in temperatures and weather patterns throughout Monterey County. The average maximum for October in the Monterey Peninsula is 70.4º and the average minimum 50.8º. It is advisable to dress in layers, with light to medium weight clothes during the day, and sweaters and jackets at night.

SYMPOSIUM HIGHLIGHTS

Technical Program:

The technical program for the 2010 IEEE CSIC Symposium consists of 54 technical papers, 4 panel sessions, an industry exhibit, and 2 short courses "High Performance Linear Transceiver MMIC Design" and "High-Speed and mm-Wave Digital-Rich Transceiver Design." We will also be offering our annual introductory level class "Basics of Compound Semiconductor ICs" (Primer Course).

This year we have invited 24 papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, we will continue the tradition of including important "late breaking news" papers.

Exciting new developments from a variety of compound semiconductor disciplines will be presented. This year there is considerable interest in GaN devices, heterogeneous integration, and radio astronomy. As always there is a tremendous amount of activity in wireless communications, as well as a strong interest in military electronics. We will have a look at the history of GaAs IC's as well as views into the future with record breaking results.

Short Course 1: "High Performance Linear Transceiver MMIC Design"

Short Course Description

As RF system requirements continue to evolve, so do the techniques and technologies for transceiver design. This course offers the student detailed instruction on circuit design fundamentals and design techniques specific to advanced technologies as well as design examples by leaders in the compound semiconductor industry.

Short Course 2: "High-Speed and mm-Wave Digital-Rich Transceiver Design"

Short Course Description

During the last 5 years, with the emergence of silicon technologies as serious contenders in wireless and wireline communication systems, we have witnessed the marriage of digital and mm-wave techniques. This change is much more radical than simply using DACs to control the bias current to calibrate the performance of high-frequency circuit blocks. This course offers the student detailed instruction on low-cost packaging techniques, circuit design fundamentals, design techniques specific to digital-rich high-frequency fiberoptics and mm-wave radio transceivers in SiGe BiCMOS and CMOS technologies.

Registration for the course is as noted in "Registration". A limited number of Short Course Notes will be available after the course for purchase by Symposium registrants, subject to availability.

Direct questions to:

Sorin Voinigescu, Short Course Coordinator
University of Toronto
(416)-946-8664
sorinv@eecg.toronto.edu

Primer Course: Basics of Compound Semiconductor ICs

The popular primer course "Basics of Compound Semiconductor ICs" is an introductory-level class intended for professionals in the electronic industry with little or no experience in compound semiconductor IC technology. It also provides an excellent review for those with more experience. The course covers: digital and analog/RF/microwave circuits; III/V materials including wide bandgap GaN and SiC; MOS and bipolar devices. The course is tailored to provide background for symposium participants to better understand and appreciate the papers presented, including a glossary of those ever-cryptic acronyms. Throughout the course, comparisons among the compound semiconductor technologies will be presented as well as comparisons with silicon technologies. Also, a number of compound semiconductor integrated circuits along with the intended applications will be described.

Instructor Donald B. Estreich has over 25 years of experience working with compound semiconductor ICs. A copy of the viewgraphs with an extensive bibliography will be distributed to each Primer Course registrant. Ample discussion time will provide an opportunity for participants to have questions answered by the instructors.

The registration fee is $175 for professionals and $100 for students. The fee includes a handout containing a copy of the overheads with an extensive reference list. Space is limited, so ADVANCE REGISTRATION IS HIGHLY RECOMMENDED.

A limited number of copies of the handouts will be available to symposium registrants, subject to availability. The cost is $50. For additional information, please contact the Primer Course Coordinator:

Direct questions to:

Douglas McPherson, Primer Course Organizer and Chair
Peraso Technologies, Inc.
120-303 Terry Fox Drive
Ottawa, ON K2K3J1, Canada
(613) 271-2020 x115 douglas@perasotech.com

Panel Sessions:

This year we have four exciting Panel Sessions spread over the 3 days of the technical sessions. These are intended to be timely, thought-provoking, educational, and hopefully controversial. The three panel topics are as follows:

PANEL SESSION 1:
"X-ParametersTM and Measurement-Based Behavioral Models: Real Models or Just Marketing?"
Monday, October 4th, 3:30-5:00 p.m.

PANEL SESSION 2:
"Ultra high-speed test and measurement, can vendors keep up and can IC developers afford it?"
Tuesday, October 5th, 1:30-3:00 p.m.

PANEL SESSION 3:
"Changing MMIC EDA Design Flows & Tools: Lessons Learned and Future Directions**"**
Tuesday, October 5th, 3:30-5:00 p.m.

PANEL SESSION 4:
"Foundry Capability and Services for Advanced III-V Processes**"**
Wednesday, October 6th, 10:30-12:00 p.m.

Please see the "Symposium Program" section later in this brochure for more complete descriptions of each of these Panel Sessions (listed according to their day and time).

Technology Exhibition:

The 2010 IEEE CSICS Technology Exhibition will be held on October 4 and 5 in De Anza I. The Exhibition is open to all Symposium registrants. The combined exhibition gives companies and attendees access to the entire array of compound semiconductor products and services, i.e., materials, manufacturing, device technology, integrated circuits, related services, commercial and military applications. Last year's exhibitors included:

Accel-RF Corporation
AWR - Applied Wave Research
EpiWorks
Sonnet Software, Inc.
Virginia Diodes Inc.
Kopin Corporation
StratEdge Corporation
Rohde & Schwarz
NNSA's National Secure Manufacturer Center
KLA-Tencor

The Exhibition will feature informative and interesting displays with corporate representatives on hand between the hours of 5:00 p.m. and 8:00 p.m. on Monday, October 4 and between 7:00 a.m. and 4:00 p.m. on Tuesday, October 5. The Exhibition will also host the Exhibition Opening Reception on Monday evening from 5:30 p.m. until 8:00 p.m. and the Exhibition Luncheon from 12:00 p.m. until 1:30 p.m. on Tuesday. All Symposium coffee breaks on Tuesday will be held in the exhibition area.

Those interested in participating in the Exhibition should contact Lukrecija Lelong, L.LeLong@ieee.org Tel: (732) 562 5441. For more information, please visit the Symposium website at http://www.csics.org/ and click on the Exhibition Information link.

Late-Breaking News Papers:

We have solicited papers containing late-breaking news for the Symposium Program. The times and locations of these presentations will be posted at the Symposium, as well as on the Symposium website.

Technical Digest:

Extra copies of the Technical Digest can be purchased by Symposium registrants through Advance Registration. A limited number of digests may also be available for sale at the Registration Desk. The cost of the paper bound digest, if ordered through Advance Registration or purchased on-site is $120. The CD ROM Digest for 2010 will also be offered for $100. Both current and past digests will be available through IEEE after the Symposium by mail from the IEEE Customer Service Center, 445 Hoes Lane, Piscataway, NJ 08854 at (800) 701-4333.

Outstanding Paper Award:

The 2010 IEEE CSIC Symposium will select a contributed paper for the Outstanding Paper Award. All contributed regular papers (not the invited papers) will automatically be considered as candidates. Symposium attendees will have an opportunity to provide feedback through a Symposium questionnaire as well as to the Session Chairpersons. The award winner will be publicly announced shortly after this year's Symposium with the award formally presented at next year's Compound Semiconductor IC Symposium

Short Courses

Sunday, October 3rd, 2010
Portola Plaza Hotel, Monterey
Bonsai I & II
8:00a.m. - 5:00p.m.

Course Coordinator: **Sorin Voinigescu**
University of Toronto
416-946-8664
sorinv@eecg.toronto.edu

"High Performance Linear Transceiver MMIC Design"

As RF system requirements continue to evolve, so do the techniques and technologies for transceiver design. This course offers the student detailed instruction on circuit design fundamentals and design techniques specific to advanced technologies as well as design examples by leaders in the compound semiconductor industry.

Topics Covered and Instructors:
1) Applications of High Linearity Transceivers – Dan Teuthorn, Endwave
2) Design of Low Phase Noise MMIC-based VCOs – Herbert Zirath, Chalmers University
3) Linear Mixer Design – Seyed Tabatabaei, Endwave
4) Phase Shifter Design – Chuck Campbell, TriQuint
5) Design of Linear PA ICs – Larry Larson, UCSD

"High-Speed and mm-Wave Digital-Rich Transceiver Design"

During the last 5 years, with the emergence of silicon technologies as serious contenders in wireless and wireline communication systems, we have witnessed the marriage of digital and mm-Wave techniques. This change is much more radical than simply using DACs to control the bias current to calibrate the performance of of high-frequency circuit blocks. This course offers the student detailed instruction on low-cost packaging techniques, circuit design fundamentals, design techniques specific to digital-rich high-frequency fiberoptics and mm-wave radio transceivers in SiGe BiCMOS and CMOS technologies.

Topics Covered and Instructors:
1) Design of High Speed ADCs and DACs – Peter Schvan, Ciena
2) Design of High Speed Serial Equalizers – Tod Dickson, IBM
3) Modulation techniques and PA requirements for High-Speed and mm-Wave Digital Rich Transceiver Design – Donald Kimball, UCSD
4) Design of mm-Wave Phased Array Building Blocks and Transceivers in Silicon - Brian Floyd, NCSU
5) Low-Cost Antenna-in-Package Development for mm-Wave Applications - Dong Kam, IBM.

Short Course Schedule

The course will be held on Sunday October 3rd and will begin with a continental breakfast. A boxed lunch will be provided as well as a morning refreshment break.

7:00 a.m. **Registration and Breakfast**

Short Course I Bonsai I

8:00 a.m. **Introduction and Overview**

8:15 a.m. **Applications of High Linearity Transceivers**
Dan Teuthorn, Endwave

9:30 a.m. **Design of Low Phase Noise MMIC-based VCOs**
Herbert Zirath, Chalmers University

10:45a.m **Coffee Break**

11:00 a.m. **Linear Mixer Design**
Seyed Tabatabaei,, Endwave

12:15 p.m. **Lunch**

1:45 p.m. **Phase Shifter Design**
Charles Campbell**,** Triquint

3:00 pm **Coffee Break**

3:15 p.m. **Design of Linear Power Amplifier ICs**
Larry Larson, UCSD

4:30 p.m. **Questions and Discussion**

5:00 p.m. **Close of Short Course**

Short Course II Bonsai II

8:00 a.m. **Introduction and Overview**

8:15 a.m. **Design of High Speed ADCs and DACs**
Peter Schvan, Ciena

9:30 a.m. **Design of High Speed Serial Equalizers**
Tod Dickson, IBM

10:45 a.m **Coffee Break**

11:00 a.m. **Modulation techniques and PA requirements for High-Speed and mm-Wave Digital Rich Transceiver Design**
Donald Kimball, UCSD

12:15 p.m. **Lunch**

1:45 p.m. **Design of mm-Wave Phased Array Building Blocks and Transceivers in Silicon**
Brian Floyd, NCSU

3:00 pm **Coffee Break**

3:15 p.m. **Low-Cost Antenna-in-Package Development for mm-Wave Applications**
Dong Kam, IBM

4:30 p.m. **Questions and Discussion**

5:00 p.m. **Close of Short Course**

Who Should Attend

The short courses are a must for everyone interested in designing advanced wireless and wireline transceivers in III-V and silicon technologies for both defense and commercial markets. Our lecturers will cater to a range of interests and experience levels. The courses are designed to give all attendees a solid overview of the design process, particularly for designing into the most advanced technologies. They will cover fundamentals, specific circuit examples and applications.

Short Course Pre-Registration

So that we may properly plan for attendance, we encourage you to pre-register for one of the two Short Courses. A limited number of short course registrations will be available on site Sunday October 3rd 7am.-8am. The registration fee is $400 for professionals and $200 for students. This includes the lectures, Notes for both Short Courses, continental breakfast, lunch, and morning/afternoon refreshments. Additional copies of the Short Course Notes may be purchased for $100 each. Registrants will be allowed to hop between the two Short Courses.

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Primer Course

Sunday, October 3rd, 2010
Portola Hotel
Bonsai III
4:00 p.m. - 7:00 p.m.

"Basics of Compound Semiconductor ICs"

Instructors: **Donald B. Estreich**
Agilent Technologies
Santa Rosa, CA

Course Coordinator: **Douglas McPherson**
Peraso Technologies, Inc.

Course Objective and Description:
The popular primer course "Basics of Compound Semiconductor ICs" is an introductory-level class intended for professionals in the electronic industry with little or no experience in compound semiconductor IC technology. It also provides an excellent review for those with more experience. The course covers: digital and analog/RF/microwave circuits; III/V materials including wide bandgap GaN and SiC; MOS and bipolar devices. The course is tailored to provide background for symposium participants to better understand and appreciate the papers presented, including a glossary of those ever-cryptic acronyms. Throughout the course, comparisons among the compound semiconductor technologies will be presented as well as comparisons with silicon technologies. Also, a number of compound semiconductor integrated circuits along with the intended applications will be described.

Instructor Donald B. Estreich each has over 25 years of experience working with compound semiconductor ICs. A copy of the viewgraphs with an extensive bibliography will be distributed to each Primer Course registrant. Ample discussion time will provide an opportunity for participants to have questions answered by the instructor.

Course Agenda:

4:00 p.m.	Introduction
4:05 p.m.	Compound Semiconductor Materials
4:30 p.m.	Device Operation
5:00 p.m.	Discussion
5:10 p.m.	Break
5:20 p.m.	Analog/RF/Microwave Circuits
6:00 p.m	RFIC Design Examples
6:40 p.m.	Summary and Discussion
7:00 p.m.	Close

The advanced registration fee is $175 for professionals and $100 for students. The fee includes a handout containing a copy of the overheads with an extensive reference list. Space is limited, so ADVANCE REGISTRATION IS HIGHLY RECOMMENDED.

A limited number of copies of the handouts will be available to symposium registrants, subject to availability. The cost is $50. For additional information, please contact the Primer Course Coordinator:

Primer Course Coordinator:
Douglas McPherson, Primer Course Organizer and Chair
Peraso Technologies, Inc.
120-303 Terry Fox Drive
Ottawa, ON K2K3J1, Canada
(613) 271-2020 x115 douglas@perasotech.com

SYMPOSIUM PROGRAM

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – De Anza Foyer
7:00 a.m. – 8:30 a.m.
Continental Breakfast – De Anza Foyer/ Lower Atrium

SYMPOSIUM OPENING

8:30 a.m. – 9:00 a.m.
De Anza III – Portola Hotel

Opening Remarks
2010 Symposium Chair
Dave Halchin, RFMD

Technical Program Overview
2010 Technical Program Chair
Dan Scherrer, Northrop Grumman

SESSION A: PLENARY SESSION

9:00 a.m. – 11:00 a.m.
De Anza III – Portola Hotel

Chairpersons: Sorin Voinigescu, *University of Toronto*
Francois Colomb, *Raytheon*

9:00 a.m.
A.1 **The Early Days of GaAs ICs (Invited)**
R.L. Van Tuyl, *Los Altos,* CA, *United States*

9:30 a.m.
A.2 **DARPAs Nitride Electronic Next Generation Technology Program (Invited)**
J.D. Albrecht[1], T. Chang[2], *[1]Defense Advanced Research Projects Agency, Arlington, United States, [2]Booz Allen Hamilton Inc., Arlington, VA, United States*

10:00 a.m.
A.3 **A Hybrid Optoelectronic Router and Enabling InP OEIC Technologies (Invited)**
R. Urata, T. Nakahara, H. Takenouchi, T. Segawa, R. Takahashi, *NTT Corporation, Atsugi, Japan*

10:30 a.m.
A.4 **The DARPA COSMOS and ELASTx Programs: Towards Next Generation Linearized Microwave/Mm-Wave Transmitters (Invited)**
S. Raman[1], T. Chang[2], I. Abdomerovic[2], C.L. Dohrman[2], M.J. Rosker[1], *[1]Defense Advanced Research Projects Agency, Arlington, VA, United States, [2]Booz Allen Hamilton Inc., Arlington, VA, United States*

11:00 a.m.
End of Session A

12:00 p.m. – 1:30 p.m.

Break for Lunch

SESSION B: Handset and Basestation Front-Ends

1:30 p.m. – 3:20 p.m.
De Anza III – Portola Hotel

Chairpersons: Karthik Krishnamurthy, *RFMD*
Tomoya Kaneko, *NEC Corporation*

1:30 p.m.
B.1 **Reconfigurable RF Front-Ends for Cellular Receivers (Invited)**
A. Mirzaei, H. Darabi, *Broadcom Corporation, Irvine, CA, United States*

2:00 p.m.
B.2 **RF Front-End Tunability for LTE Handset Applications (Invited)**
R. B. Whatley, T. Ranta, D. J. Kelly, *Peregrine Semiconductor, San Diego, CA, United States*

2:30 p.m.
B.3 **Doherty Power Amplifiers using 2nd Generation HVHBT Technology for High Efficiency Basestation Applications (Invited)**
C. Steinbeiser, P. Page, T. Landon, G. Burgin, *TriQuint Semiconductor, Richardson, TX, United States*

3:00 p.m.
B.4 **Design and Characterizations of a Novel Vertical Transistor for Long- Pulse RF Power Amplification**
W. Cai, D. Rice, B. P. Gogoi, P. Le, D. Lutz, *HVVi Semiconductors, Phoenix, AZ, United States*

3:20 p.m.
End of Session B

SESSION C: GaN HEMT Modeling

1:30 p.m. – 3:10 p.m.
De Anza II – Portola Hotel

Chairpersons: Joe Gering, *RFMD*
Wolfram Stiebler, *TriQuint Semiconductor*

1:30 p.m.
C.1 **AlGaN/GaN HFET Models and the Prospects for Physics-Based Compact Models (Invited)**
R. J. Trew, *North Carolina State University, Raleigh, NC, United States*

2:00 p.m.
C.2 **GaN Device Modeling with X-parameters (Invited)**
J. Horn[1], G. Simpson[2] , D. E. Root[1], *[1]Agilent Technologies, Santa Rosa, CA, United States, [2]Maury Microwave, Ontario CA, , United States*

2:30 p.m.

C.3 **A Scalable and Distributed Electro-thermal Model of AlGaN/GaN HEMT Dedicated to Multi-Fingers Transistors**
A. Xiong, C. Charbonniaud, E. Gatard, S. Dellier, *AMCAD Engineering, Limoges, France*

2:50 p.m.
C.4 **A Verilog-A Large-Signal GaN HEMT Model for High Power Amplifier Design**
F. Kharabi, J. McMacken, J. Gering, *RFMD, Greensboro, NC, United States*

3:10 p.m.
End of Session C

3:10 p.m. – 3:30 p.m.
Coffee Break

SESSION D: High Speed Digital Circuits

3:30 p.m. – 4:50 p.m.
De Anza III – Portola Hotel

Chairpersons: Peter Schvan, *Ciena*
Greg Creech, *AFRL*

3:30 p.m.
D.1 **A 204.8 GHz Static Divide-by-8 Frequency Divider in 250 nm InP HBT**
Zach Griffith[1], Miguel Urteaga[1], Richard Pierson[1], Petra Rowell[1], Mark Rodwell[2], Bobby Brar[1], [1]*Teledyne Scientific Company, Thousand Oaks, CA, United States,* [2]*University of California Santa Barbara, Santa Barbara, CA, United States*

3:50 p.m.
D.2 **A 4x28.3 Gb/s SFI-S SerDes in 130 nm SiGe (Invited)**
Thomas Krawczyk, Todd Cooper, Samuel Steidl, Peter Curran, Massashi Yamagata, Song Shang, Tony Liu, Cliff Duong, Zuoding Wang, Kun-Wook Chung, Craig Hornbuckle, David Rowe, *Semtech Corporation, Camarillo,CA, United States*

4:20 p.m.
D.3 **A 40 Gb/s Multi-Data-Rate CMOS Transmitter and Receiver Chipset with SFI-5 Interface for Optical Transmission Systems (Invited)**
Hidemi Noguchi[1], Tomoyuki Yamase[1], Kenchi Hosoya[1], Minoru Okamoto[3], Hiroshi Yamaguchi[4], Hiroaki Shoda[4], Risato Ohhira[2], Arihide Noda[1], Sadao Fujita[1], Nobuhiro Kawahara[5], [1]*NEC Corporation, Kawasaki, Kanagawa, Japan,* [2]*NEC Corporation, Sagamihara, Japan,* [3]*NEC Engineering Ltd, Kawasaki, Japan,* [4]*NEC Corporation, Fuchu, Tokyo, Japan,* [5]*NEC Corporation, Abiko, Japan*

4:50 p.m.
End of Session D

PANEL SESSION 1:

X-Parameters™ and Measurement-Based Behavioral Models: Real Models or Just Marketing?

3:30 p.m. – 5:00 p.m.
De Anza II – Portola Hotel

Moderators: Joe Gering, *RFMD*
Seyed Tabatabaei, *EndWave Corporation*

Designers have been using S-parameters and parameterized device models for decades to do RF design with good success. Recently, the industry has seen the introduction of nonlinear parameters / behavioral models for example X-parameters™, S-functions, and the Cardiff model. In many ways, this amount to a brute force look-up table that has been indexed over a large array of large-signal operating points and either interpolates large-signal behavior or linearizes small-signal perturbations. While this has been demonstrated for finished amplifiers, where the operating conditions are manageable, it seems to be awkward for device-level models where the parameter space is much broader (for example frequency, drain/collector bias, gate/base bias, temperature, load impedance, source impedance, etc.). Are these measurement based behavioral models the next wave in modeling or just another tool in the toolbox? Questions for this panel include:

- Do these measurement-based behavioral models provide any better solution compared to the use of conventional compact modeling approaches?
- What is the cross-over point in part complexity for measurement based behavioral models?
- Is it better to have a device equivalent circuit model that works over all operating conditions with reasonable accuracy or a measurement based behavioral model that is very accurate over a limited range?
- How do you come up with a measurement based model when you have nothing to measure?
- How does convergence and simulation speed for measurement based models compare to traditional approaches?
- Does the high cost of the measurement systems require to generate these models make their use viable?
- The measurement approach and model were initially a one-company show. How well is this technology being propagated to other equipment and software vendors?

Panel Members:

David Root	X-parameter Model	*Agilent Technologies*
Paul Tasker	Cardiff Model	*Cardiff University*
Mike Golio	Compact Model	*Golio Consulting*
Yusuke Tajima	Modeling Services	*Auriga Microwave*
Gayle Collins	Design/User	*Freescale Semiconductor*
Ed Anthony	Design/User	*Skyworks Solutions*

5:00 p.m.
End of Panel Session 1

Monday, October 4th, 2010

Technology Exhibition
Opening Reception
De Anza I
Portola Hotel
5:30 p.m. - 8:00 p.m.

Tuesday, October 5th, 2010

REGISTRATION AND BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – De Anza Foyer
7:00 a.m. – 8:30 a.m.
Continental Breakfast – De Anza I

SESSION E: Ultra Low Noise Receivers for Radio Astronomy

8:30 a.m. – 9:50 a.m.
De Anza III – Portola Hotel

Chairpersons: Herbert Zirath, *Chalmers University*
Gilberto De la Rosa, *Anadigics Inc*

8:30 a.m.
E.1 **Receiver Integration for Mid-band Square Kilometer Array Demonstrator Applications (Invited)**
S. A. Jackson[1], R. G. Gough[1], Y. Moghe[2]
[1]Commonwealth Scientific and Industrial Research Organization, Marsfield, Australia, [2]Sapphicon Semiconductor, Homebush, Australia

9:00 a.m.
E.2 **Front-end Integration Requirements for the Square Kilometre Array Radio Telescope (Invited)**
J.G. Bij de Vaate, R.H. Witvers, E.E.M. Woestenburg
ASTRON, Dwingeloo, The Netherlands

9:30 a.m.
E.3 **A Low Noise Integrated 0.3-20 GHz Differential Amplifier for Balanced Ultra Wideband Antennas**
N. Wadefalk , P.S. Kildal, H. Zirath
Chalmers University of Technology, Göteborg, Sweden,

9:50 a.m.
E.4 **LNA Design Based on an Extracted Single Gate Finger Model**
S. J. Mahon[1], A. Dadello[1], P. Vun[1], J. Tarazi[2], A. C. Young[1], M. C. Heimlich[2], J. T. Harvey[1], A. E. Parker[2], [1]Mimix Broadband, North Sydney, Australia, [2]Macquarie University, Macquarie University, Australia

10:10 a.m.
End of Session E

SESSION F: III-V Advanced IC Technology

8:30 a.m. – 10:00 a.m.
De Anza II

Chairpersons: Martin Dvorak, *Agilent Technologies*
Nils Weimann, *Alcatel-Lucent Bell Labs*

8:30 a.m.
F.1 **InP HBT Integrated Circuit Technology for Terahertz Frequencies (Invited)**
M. Urteaga[1], R. Pierson[1], J. Hacker[1], M. Seo[1], Z. Griffith[1], A. Young[1], P. Rowell[1], and M.J.W. Rodwell[2]
[1]Teledyne Scientific Company, Thousand Oaks, CA, USA
[2]ECE Department, UC Santa Barbara, CA, USA

9:00 a.m.
F.2 **A Low 1/*f* Noise and High Reliability InP/GaAsSb DHBT for 76 GHz Automotive Radars**
K. Kanaya, H. Amasuga, S. Watanabe, Y. Yamamoto, N. Kosaka, S. Miyakuni, S. Goto, and A. Shima, *High Frequency and Optical Device Works. Mitsubishi Electric Corporation, Hyogo, Japan*

9:20 a.m.
F.3 **75 GHz Ga_2O_3/GaN Single Nanowire Metal-Oxide-Semiconductor field-effect Transistors**
Jeng-Wei Yu, Yuh-Renn Wu, Jian-Jang Huang, and Lung-Han Peng, *Institute of Photonics and Optoelectronics and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C.*

9:40 a.m.
F.4 **Development of 90 nm InGaAs HEMTs and Benchmarking Logic Performance with Si CMOS**
Kuang-Yu (Donald) Cheng[1], Doris Chan[1], Fei Tan[1], Huiming Xu[1], Milton Feng[1], Chih-Hsin Ko[2] and Clement Wann[2], *[1]Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL, USA [2]Exploratory Technology Development Department, Taiwan Semiconductor Manufacturing Company (TSMC), HsinChu, Taiwan*

10:00 a.m.
End of Session F

10:00 a.m. - 10:30 a.m.
Coffee Break

SESSION G: Digital and Optoelectronic Systems

10:30 a.m. – 12:00 p.m.
De Anza III – Portola Hotel

Chairpersons: Kimikazu Sano, *NTT*
Y.K. Chen, *Alcatel-Lucent*

10:30 a.m.
G.1 **Compacting High-End Computing Systems with Dense, Wavelength-Division Multiplexed Silicon Photonic Interconnects (Invited)**
A. V. Krishnamoorthy, J. E. Cunningham, *Sun Labs, Oracle, San Diego, CA, United States*

11:00 a.m.
G.2 **32 GS/s Soft Decision LSI in 0.13 um SiGe BiCMOS for Forward Error Correction in Optical Communications (Invited)**
T. Kobayashi, S. Kametani, H. Tagami, K. Koguchi, T. Mizuochi, *Mitsubishi Electric Corporation, Ofuna, Japan*

11:30 a.m.
G.3 **InP IC Technology Powers Agilent's 90000X Series Real Time Oscilloscope Family (Invited)**
Robert Shimon[3], Brig Asay[1], Dave Dascher[1], Keith Grigs[2], Chris Rehorn[2], Miroslaw Adamski[3], Eric Ehlers[3], Craig Hutchinson[3], Brad Doerr[1], *[1]Agilent Technologies, Inc., Digital Test Division, Colorado Springs, CO, United States, [2]Agilent Technologies, Inc., Technology Leadership Organization, Colorado Springs, CO, United States, [3]Agilent Technologies, Inc., Technology Leadership Organization, Santa Rosa, CA, United States*

12:00 p.m.
End of Session G

SESSION H: III-V/Silicon Heterogeneous Integration

10:30 a.m. – 12:20 p.m.
De Anza II – Portola Hotel

Chairpersons: Jim Sewell, *AFRL*
Brian Moser, *RFMD*

10:30 a.m.
H.1 **High Performance Mixed Signal Circuits Enabled by the Direct Monolithic Heterogeneous Integration of InP HBT and Si CMOS on a Silicon Substrate (Invited)**
T.E. Kazior[1], J.R. LaRoche[1], D. Lubyshev[2], J.M. Fastenau[2], W.K. Liu[2], M. Urteaga[3], J. Bergman[3], M.J. Choe[3], K.J. Lee[3], T. Seong[3], M. Seo[3], A. Yen[3], M.T. Bulsara[4], E.A. Fitzgerald[4], D. Smith[5], D. Clark[5], R. Thompson[5], C. Drazek[6], E. Guiot[6], *[1]Raytheon Integrated Defense Systems, Andover MA, United States, [2]IQE Inc. Bethlehem PA, United States, [3]Teledyne Scientific Company, Thousand Oaks, CA, United States, [4]Massachuessetts Institute of Technology, Cambridge, MA, United States, [5]Raytheon Systems Limited, Glenrothes, United Kingdom, [6]SOITEC Bernin, France*

11:00 a.m.
H.2 **Advanced Heterogeneous Integration of InP HBT and CMOS Si Technologies (Invited)**
Augusto Gutierrez-Aitken, Patty Chang-Chien, Dennis Scott, Kelly Hennig, Eric Kaneshiro, Peter Nam, Neir Cohen, Daniel Ching, Khanh Thai, Bert Oyama, Joe Zhou, Craig Geiger, Ben Poust, Matthew Parlee, Randy Sandhu, Wen Phan, Aaron Oki, Reynold Kagiwada, *Northrop Grumman Aerospace Systems, Redondo Beach, CA, United States*

11:30 a.m.
H.3 **Mixed-Signal Circuits Using 250nm InP HBT Technology Integrated with 90nm CMOS (Invited)**
K. R. Elliott, *HRL Laboratories LLC, Malibu, CA, United States*

12:00 p.m.
H.4 **Monolithically-Integrated Digital Circuits with Light Emitting Diodes in Lattice-Matched Si/III-V-N/Si Heterostructure**
Akihiro Wakahara, Keisuke Yamane, Kenta Noguchi, Seizo Tanaka, Yuzo Furukawa, Hiroshi Okada, Hiroo Yonezu *Toyohashi University of Technology, Toyohashi, Japan*

12:20 p.m.
End of Session H

12:00 p.m. – 1:30 p.m.
Break for Lunch

Technology Exhibition Lunch
De Anza I
Portola Hotel
12:00 p.m. – 1:30 p.m.

PANEL SESSION 2:
Ultra high-speed test and measurement, can vendors keep up and can IC developers afford it?

1:30 p.m. – 3:00 p.m.
De Anza II – Portola Hotel

Moderators: Cynthia Baringer, *HRL Laboratories*
Peter Cheng, *Northrop Grumman*

The emergence of ultra-high-speed communications circuits presents a significant challenge for IC developers and test equipment vendors. While the technology and tools exist for designing >25 GS/s ADC/DACs, and >40 Gb/s serial transceivers, test and measurement equipment for verifying their performance is nearly non-existent. With many of these new ICs pushing high speed, low-noise, and high-precision to the limit, can test and measurement equipment actually measure them? If so, what would such equipment cost and can IC design shops, many of them start-ups, even begin to afford it? This panel session will bring together ultra-high-speed IC designers and test and measurement experts from the leading vendors. The aim is to clearly articulate the challenges and requirements of the designers and what the test and measurement vendors are doing to address them.

Panel Members:

Ken Nishimura	Vendor	*Agilent Technologies*
Eric Strid	Vendor	*Cascade Microtech*
Julio Perdomo	Vendor	*Centellax*
Martin Murphy	Vendor	*Anritsu*
Peter Schvan	End User	*Ciena*
Ken Elliott	End User	*HRL Laboratories*

3:00 p.m.
End of Panel Session 2

3:00 p.m. - 3:30 p.m.
Coffee Break

Tuesday, October 5th, 2010

PANEL SESSION 3:
Changing MMIC EDA Design Flows & Tools: Lessons Learned and Future Directions

3:30 p.m. – 5:00 p.m.
De Anza III – Portola Hotel

Moderators: Steve Brown, *TriQuint*
Jim Carroll, *AWR*

Back in the late '90s, the DARPA MAFET program wanted a "threefold design cost and cycle-time reduction goal" with a vision of totally synchronized layouts, integrated flows, and EM simulations of entire MMICs and Modules. Currently, RF design circuit size and cycle time requirements are getting smaller and shorter while required circuit complexity and functionality is getting larger. The CAE tools need to keep moving forward to match. Panelist will review where we were 15 years ago, where their products are now, and what they see are future industry trends. They will help answer what are the current typical design hurtles and where the EDA industry can help make designers more productive, faster, and overall designs better.

Panel Members:

Greg Creech	Deputy AF MAFET Program Manager
Ted Miracco	AWR
Todd Cutler	Agilent
Scott Wedge	Synopsis
John Pierce	Cadence
Mike Heimlich	Macquarie University

5:00 p.m.
End of Panel Session 3

SESSION I: High Speed & mm-Wave CMOS

3:30 p.m. – 5:15 p.m.
De Anza II – Portola Hotel

Chairpersons: Jonghae Kim, *Qualcomm Incorporated*
Payam Heydari, *University of California at Irvine*

3:30 p.m.
I.1 **An 8.2 to 20.1GHz LC PLL with Sub-100fs Jitter in 0.13um SiGe BiCMOS**
Murat Demirkan, Günter Steinbach, Ken A. Nishimura, John P. Keane, Bernd E. Wüppermann, *Agilent Technologies, Santa Clara, CA, United States*

3:55 p.m.
I.2 **A CMOS Programmable Gain Amplifier with Constant Current-Density Based Transconductance Control**
So Young Kang, Seung Tak Ryu, Chul Soon Park, *KAIST, Korea*

4:20 p.m.

Tuesday, October 5th, 2010

I.3 **A 80-92-GHz Receiver Front-End using Slow-Wave Transmission Lines in 65nm CMOS**
Chun-Cheng Wang[1], Zhiming Chen[1], Vipul Jain[2], Payam Heydari[1], *[1]University of California, Irvine, CA, [2]Saber Tek Inc., Irvine, United States*

4:45 p.m.
I.4 **Gbps 60GHz CMOS OOK Modulator and Demodulator**
Jae Jin Lee, Chul Woo Byeon, Ki Chan Eun, Inn Yeal Oh, Chul Soon Park, *KAIST, Korea*

5:15 p.m.
End of Session I

Symposium Theme Party
"CSICS: Back in the Bay"
Memory Gardens
6:00 p.m. - 10:00 p.m.

Wednesday, October 6th, 2010

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 2:00 p.m.
Registration – De Anza Foyer
7:00 a.m. – 8:30 a.m.
Continental Breakfast – De Anza Foyer/ Lower Atrium

SESSION J: Power and Switching GaN Devices

8:30 a.m. – 10.00 a.m.
De Anza III – Portola Hotel

Chairpersons: Toshi Kikkawa, *Fujitsu Laboratories*
Rik Jos, *NXP Semiconductors*

8:30 a.m.
J.1 **Soft Switching Controlled AlGaN Based Power Transistors for Induction Heating Applications**
Y. Niiyama[1], M. Masuda[2], N. Ikeda[1], S. Kato[1], *[1]Advanced Power Device Research Association, Yokohama, Japan, [2]R&D Center of Advanced Automotive & Electronics, Furukawa Electric, Kanagawa, Japan*

8.50 a.m.
J.2 **Recent Advances in GaN Power Switching Devices (Invited)**
Satoshi Tamura[1], Yoshiharu Anda[1], Mashahiro Ishida[1], Yasuhiro Uemoto[2] , Tetsuzo Ueda[1], Tsuyoshi Tanaka[1], Daisuke Ueda[3], *[1]Semiconductor Device Research Center, Panasonic Corporation, Kyoto, Japan, [2]Discrete Device Development Center, Panasonic Corporation, Kyoto, Japan, [3]Advanced Technology Research Laboratories, Panasonic Corporation, Kyoto, Japan,*

9.20 a.m.
J.3 **Developing GaN HEMTs for Ka-Band with 20W**
Kazutaka Takagi[1], Keiichi Matsushita[1], Yasushi Kashiwabara[1], Kazutoshi Masuda[1], Shinichiro Nakanishi[1], Hiroyuki Sakurai[1], Ken Onodera[1], Hisao Kawasaki[1], Yoshiharu Takada[2], Kunio Tsuda[2], *[1]Microwave Solid-State Engineering Dept., Toshiba Corporation, Kawasaki, Japan, [2]Electron Device Laboratory, Corporate R&D Center, Toshiba Corporation, Kawasaki, Japan*

9.40 a.m.
J.4 **S-parameter Analysis of GaN Schottky Diodes for Microwave Power Rectification**
Jing-Ping Ao[1], Kensuke Takahashi[1], Naoki Shinohara[2], Naoki Niwa[3], Teruo Fujiwara[4], Yasuo Ohno[1], *[1]Institute of Technology and Science, University of Tokushima, [2]Research Institute for Sustainable Humanosphere, Kyoto University, [3]Kajima Technical Research Center, Kajima Corporation, [4]Sho Engineering Corporation, Japan*

10.00 a.m.
End of Session J

SESSION K: mm-Wave Oscillators and Phase

Shifters

8:30 a.m. – 9:50 a.m.
De Anza II – Portola Hotel

Chairpersons: Seyed Tabatabaei, *Endwave Corp.*
Val Kaper, *Raytheon*

8:30 a.m.
K.1 **An InP VCO with Static Frequency Divider for Millimeter Wave Clock Generation**
M. Stuenkel, M. Feng, *University of Illinois at Urbana-Champaign, Urbana, IL, United States*

8:50 a.m.
K.2 **An mHEMT Q-Band Integrated LNA and Vector Modulator MMIC**
J. Lynch, F. A. Traut, K. Benson, R. Tshudy, *Hittite Microwave Corp., Chelmsford, MA, United States*

9:10 a.m.
K.3 **Design and characterization of a V-Band Quadrature VCO based on a Common-Collector SiGe Colpitts VCO**.
A.Barghouthi[1], A. Krause[1], C. Carta[1], F. Ellinger[1], C. Scheytt[2],[1]*Dresden University of Technology, Dresden, Germany,* [2]*IHP GmbH, Frankfurt (Oder), Germany*

9:30 a.m.
K.4 **Voltage-controlled Phase Shifter in a Surface Mount Package for 40- and 100-Gb/s Optical Transceivers**
H. Nosaka, M. Nagatani, K. Sano, T. Ito, S. Tsunashima, K. Murata, *NTT Corporation, Atsugi, Japan*

9:50 a.m.
End of Session K

10:00 a.m. - 10:30 a.m.
Coffee Break

PANEL SESSION 4:
Foundry Capability and Services for Advanced III-V Processes

10:30 a.m. – 12:00 p.m.
De Anza III

Moderators: Mike Wojtowicz, *Northrop Grumman*
Martin Dvorak, *Agilent Technologies*

In the Silicon world, wafer fabrication is a commodity. The foundry provides well-proven models, and delivers on a relatively tight set of specifications. Competing foundries can even be depended upon to produce parts that are mutually functionally interchangeable. But for advanced III-V technologies such as InP HBT and GaN, on which exciting new ICs are fabricated and routinely reported on at conferences such as CSICS, such an infrastructure is still in relative infancy.

The panelists will present from either the point of view of purveyors of foundry services and/or from the point of view of their customers:

Wednesday, October 6th, 2010

Why can't you give an accurate device and interconnect model? What is the reliability of the device, the interconnects, and the interlayer dielectric? Will the same process be available next year/next month? How about uniformity and repeatability? Can you predict the next time you will be making an order for parts, and how many you'll need? Can you design according to the design guidelines or must you insist on trying stupid interconnect or device tricks on the same wafer as real ICs? How about some feedback on how the parts we delivered fared in your tests?

Panel Members:

Tony Balistreri	vendor	*TriQuint Semiconductor*
Tom Joseph	vendor	*RFMD*
Wing Yao	vendor	*GCS*
Perry Tapp	middle-man	*Kansas City Plant*
Seyed Tabatabaei	end user	*Endwave Technologies*
Vinny Cannistraro	end user	*Hittite*

12:00 p.m.
End of Panel Session 4

SESSION L: Power Amplifiers for Microwave and MMW Applications

10:30 a.m. – 12:00 p.m.
De Anza II – Portola Hotel

Chairpersons: Steve Brown, *TriQuint Semiconductor*
Harris Moyer, *HRL Laboratories LLC*

10:30 a.m.
L.1 **An X-Band 50W-output/30%-PAE GaN Power Amplifier with Bandwidth/Ripple-Optimized Bandpass Impedance-Matching Networks**
H. Uchida, E. Kuwata, H. Ohtsuka, K.Yamanaka, K. Yamauchi, K. Mori, M. Nakayama, A. Inoue, and Y. Hirano, *Mitsubishi Electric Corporation, Kamakura, Japan*

10:50 a.m.
L.2 **Design and Performance of a High Efficiency Ka-band Power Amplifier MMIC**
C. F. Campbell, D. C. Dumka, M. Y. Kao, D. M. Fanning, *TriQuint Semiconductor, Richardson, TX, United States*

11:10 am.
L.3 **Scaling of InP HEMT Cascode Integrated Circuits to THz Frequencies**
W. Deal, K. Leong, X.B. Mei, S. Sarkozy, V. Radisic, J. Lee, P. H. Liu, W. Yoshida, J. Zhou, M. Lange. *Northrop Grumman Corporation, Redondo Beach, CA, United States*

11:30 p.m.
L.4 **E-band 85-mW Oscillator and 1.3-W Amplifier ICs using 0.12-um GaN HEMTs for Millimeter-wave Transceivers**
Y. Nakasha[1], S. Masuda[1], K. Makiyama[1], T. Ohki[1], M. Kanamura[1], N. Okamoto[1], T. Tajima[1], T. Seino[1], H. Shigematsu[1], K. Imanishi[1], T. Kikkawa[1], K. Joshin[1], N. Hara[2], [1]*Fujitsu Limited, Atsugi, Japan,* [2]*Fujitsu Laboratories Ltd., Atsugi, Japan*

12:00 p.m.

End of Session L

12:00 p.m. – 1:30 p.m.
Break for Lunch

SESSION M: GaN and GaAs HFETs

1:30 p.m. – 3:20 p.m.
De Anza III – Portola Hotel

Chairpersons: Marc Rocchi, *Ommic*
Ming-Yih Kao, *TriQuint Semiconductor*

1:30 p.m.
M.1 **Microwave GaN HEMT Reliability Observations (Invited)**
S. C. Binari[1], J. A. Mittereder1[1], and G. D. Via[2],
[1] Naval Research Laboratory, Washington DC, United States, [2] Air Force Research Laboratory, Wright Patterson AFB, OH, United States

2:00 p.m.
M.2 **Single-Polarity Power Supply Bootstrapped Comparator for GaN Smart Power Technology**
Xiaosen Liu and Kevin J.Chen,
Hong Kong University of Science and Technology, Hong Kong

2:20 p.m.
M.3 **Comparative Study of AlGaN/GaN HEMTs on Free-Standing Diamond and Silicon Substrates for Thermal Effects**
Manuel Trejo[1], Kelson D. Chabak[1], Brain Poling[1], Ryan Gilbert[1], Antonio Crespo[1], James K.Gillespie[1], Mauricio Kossler[1], Dennis E. Walker[1], Glen D. Via[1], Gregg H. Jessen[1], Daniel Francis[2], Firooz Faili[2], Dubravko Babié[2], and Felix Ejeckam[2],
[1] Air Force Research Laboratory, Dayton, OH, United States, [2] Group4 Labs, Inc., Fremont, CA, United States

2:40 p.m.
M.4 **Advanced Full Periphery pHEMT Switch with Optimum Figure of Merit Ron*Coff**
Cheng-Guan Yuan, S.M. Joseph Liu, and Shinichiro Takatani,
WIN Semiconductors Corp., Taiwan

3:00 p.m.
M.5 **Development of Ka-band GaAs pHEMTs with Output Power over 1 W/mm**
Deep C. Dumka, Ming-Yih Kao, Edward Beam, Tso-Min Chou, Hua-Quen Tserng, and David M. Fanning,
TriQuint Semiconductor, Richardson, TX, United States

3:20 p.m.
End of Session M

SESSION N: mm-Wave to THz Mixing Technologies

1:30 p.m. – 2:30 p.m.

Wednesday, October 6th, 2010

De Anza II – Portola Hotel

Chairpersons: Kazuya Yamamoto, *Mitsubishi Electric Corp.*
Michael Heimlich, Macquarie University

1:30 p.m.
N.1 **Packaged, Integrated 32 to 40 GHz Millimetre-Wave Up-Converter**
Emmanuelle R.O. Convert, Anthony P. Fattorini, Simon J. Mahon, P.W. Evans, M.G. McCulloch, S. Hwang, Rodney G. Mould, Alan C. Young, and James T. Harvey, *Mimix Broadband, North Sydney, Australia*

1:50 p.m.
N.2 **Subharmonically Pumped 210 GHz I/Q Mixers**
D. Lopez-Diaz, I. Kallfass, A. Tessmann, A. Leuther, H. Massler, M. Schlechtweg, O. Ambacher, *Fraunhofer Institute for Applied Solid State Physics IAF, Freiburg, Germany*

2:10 p.m.
N.3 **A Fundamental Upconverting Gilbert Mixer for 100 GHz Wireless Applications**
Marcus Gavell[1], Mattias Ferndahl[1], Herbert Zirath[1], Miguel Urteaga[2], Richard Pierson[2], *[1] Chalmers University of Technology, Microwave Electronics Laboratory, Gőteborg, Sweden, [2] Teledyne Scientific Company, Thousand Oaks, CA, United States.*

2:30 p.m.
End of Session N

3:00 p.m. – 3:30 p.m.
Coffee Break

SESSION O: Late News Papers

3:30 p.m. – 4:30 p.m.
De Anza III

Chairpersons: Dave Halchin, *RFMD.*
Dan Scherrer, *Northrop Grumman*

3:30 p.m.
O.1 **RF Receiver Front End for 868.6-MHz Band IEEE 802.15.4 PSSS Standard**
S. M. Anis[1], G. Grau[2], *[1] University of Ulm, Ulm, Germany, [2] ADvico , Recklinghausen, Germany*

3:50 p.m.
O.2 **A 0.1-1.8 GHz, 100 W GaN HEMT Power Amplifier Module**
K. Krishnamurthy, D. Lieu, R. Vetury, J. Martin, *RFMD, Charlotte, United States*

4:10 p.m.
O.3 **A Metamorphic HEMT S-MMIC Amplifier with 16.1 dB Gain at 460 GHz**
A. Tessmann, A. Leuther, R. Loesch, M. Seelmann-Eggebert, H. Massler, *Fraunhofer IAF, Freiburg, Germany*

4:30 p.m.
End of Session O

Wednesday, October 6th, 2010

SESSION P: Late News Papers

3:30 p.m. – 4:30 p.m.
De Anza II

Chairpersons: Douglas S. McPherson, *Peraso Technologies Inc.*
Charles Campbell, *TriQuint Semiconductor*

3:30 p.m.
P.1 **A 56 Gbit/s 0.35 µm SiGe Limiting Amplifier with 2.4 THz Gain-Bandwidth-Product**
M. Groezing, M. Schmidt, M. Berroth, *University of Stuttgart, Stuttgart, Germany*

3:50 p.m.
P.2 **A 2.4 Vpp, 60-Gb/s, mm-Wave DAC-based CMOS Driver with Adjustable Amplitude and Peaking Frequency**
R. A. Aroca[1], S. P. Voinigescu[1], P. Schvan[2], *[1]University of Toronto, Toronto, Canada, [2]Ciena, Ottawa, Canada*

4:10 p.m.
P.3 **An Ultrahigh-Speed Low-Power DAC using InP HBTs for Multi-Level Optical Transmission Systems**
M. Nagatani[1], H. Nosaka[1], S. Yamanaka[2], K. Sano[1], K. Murata[1], *[1]NTT Corporation, Atsugi, Japan, [2]NTT Corporation, Yokosuka, Japan*

4:30 p.m.
End of Session P

Close of Symposium

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