39th IEEE COMPOUND SEMICONDUCTOR IC (CSIC) SYMPOSIUM

Program

Presenting:

The Sun sets on CSICS!!

Oct 22nd – Oct 25th, 2017
Miami Marriott Biscayne Bay
Miami, Florida
USA

CO- SPONSORED BY
The IEEE Electron Devices Society,
The IEEE Solid-State Circuits Society, and
The IEEE Microwave Theory and Techniques Society.

SYMPOSIUM

Sunday, October 22nd, 2017
REGISTRATION for Short Course and Primer
Short Course/Primer Continental Breakfast
SHORT COURSE: Silicon Photonics Technology and Design
PRIMER 1: Introduction to MMIC High Power Amplifier Design
PRIMER 2: Introduction to Si RF and Mixed Signal IC Design
Short Course Lunch
REGISTRATION for Symposium
CSIC Symposium Opening Cocktails

Monday, October 23rd, 2017
REGISTRATION
Continental Breakfast
SYMPOSIUM OPENING
SESSION A: Plenary Session
SESSION B: GaN-Based Systems and Components
SESSION C: Characterization and Analysis of HBTs
PANEL SESSION 1: Optics Invading Copper? The Future of Backplane Communication
Exhibition Opening Reception
Technology Exhibition

Tuesday, October 24th, 2017
REGISTRATION
Technology Exhibition
Exhibition Breakfast
SESSION D: High Speed Serial Links
SESSION E: Advanced Devices and Modeling
SESSION F: Advancements of mm-Wave & THz
SESSION G: GaN Devices are Muy Caliente: Thermal Characterization of GaN HEMTs
Exhibition Lunch
SESSION H: III/V Solutions for 5G Applications
SESSION I: GaN HEMT Modeling for Amplifier Design
PANEL SESSION 2: Have North America and Europe handed the Semiconductor Industry to ASIA?

Wednesday, October 25th, 2017
REGISTRATION
Continental Breakfast
SESSION J: THz Systems and Applications
SESSION K: Next Generation Wide Bandgap Technologies
SESSION L: RF Front End Control Circuits
SESSION M: Photonic Integrated Circuits
SESSION N: High-Performance Circuits for Digital Communications
SESSION O: Late-Breaking News Papers I
SESSION P: Late-Breaking News Papers II

Close of Symposium

AT A GLANCE

Sunday, October 22nd, 2017

7:00 a.m. – 8:00 a.m.	3rd Floor Foyer (Registration for Short Course and Primer)
7:00 a.m. – 8:00 a.m.	**Bayview Ballroom (Breakfast)**
8:00 a.m. – 5:50 p.m.	Watson (Short Course)
8:00 a.m. – 9:30 a.m.	Hibiscus (Primer 1)
10:00 a.m. – 7:00p.m.	Hibiscus (Primer 2)
12:00 p.m. – 1:00 p.m.	**Bayview Ballroom (Lunch)**
3:00 p.m. – 8:00 p.m.	3rd Floor Foyer (Registration for Symposium)
7:00 p.m. – 8:00 p.m.	**Bayview Ballroom (Cocktails)**

Monday, October 23rd, 2017

7:00 a.m. – 5:00 p.m.	3rd Floor Foyer (Registration)
7:00 a.m. – 8:15 a.m.	**Salon F (Breakfast)**
8:15 a.m. – 8:45 a.m.	Salon E (Symposium Opening)
8:45:00 a.m. – 12:00 p.m.	Salon E (Plenary)
1:30 p.m. – 3:00 p.m.	Salon E (Session B)
1:30 p.m. – 3:00 p.m.	Salon ABCD (Session C)
3:30 p.m. – 5:00 p.m.	Salon E (Panel 1)
5:30 p.m. – 7:30 p.m.	**Salon F (Exhibition)**
5:30 p.m. – 7:30 p.m.	**Salon F (Reception)**

Tuesday, October 24th, 2017

7:00 a.m. – 5:00 p.m.	3rd Floor Foyer (Registration)
7:30 a.m. – 3:30 a.m.	**Salon F (Exhibition)**
7:30 a.m. – 8:30 a.m.	**Salon F (Exhibition Breakfast)**
8:30 a.m. – 9:50 a.m.	Salon E (Session D)
8:30 a.m. – 9:50 a.m.	Salon ABCD (Session E)
10:30 a.m. – 11:40 p.m.	Salon E (Session F)
10:30 a.m. – 11:40 p.m.	Salon ABCD (Session G)
12:00 p.m. – 1:30 p.m.	**Salon F (Exhibition Luncheon)**
1:30 p.m. – 3:00 p.m.	Salon E (Session H)
1:30 p.m. – 2:40 p.m.	Salon ABCD (Session I)
3:30 p.m. – 5:00 p.m.	Salon E (Panel 2)
6:00 p.m. – 10:00 p.m.	Biscayne Lady Sunset Cruise Party

Wednesday, October 25th, 2017

7:00 a.m. – 12:00 p.m.	3rd Floor Foyer (Registration)
7:00 a.m. – 8:30 a.m.	**Salon F (Breakfast)**
8:30 a.m. – 9:50 a.m.	Salon E (Session J)
8:30 a.m. – 9:40 a.m.	Salon ABCD (Session K)
10:30 a.m. – 12:00 p.m.	Salon E (Session L)
10:30 a.m. – 11:50 p.m.	Salon ABCD (Session M)
1:30 p.m. – 2:40 p.m.	Salon E (Session N)
1:30 p.m. – 3:10 p.m.	Salon ABCD (Late-Breaking Papers I)
3:30 p.m. – 5:15 p.m.	Salon E (Late-Breaking Papers II)

5:15 p.m. End of Symposium

Visit us at: http://www.csics.org

CHAIR'S MESSAGE

It is with great pleasure that I invite you to be a part of the 2017 IEEE Compound Semiconductor IC Symposium (CSICS). For our 39th year, CSICS will be held on Sunday October 22 to Wednesday October 25 in Miami, Florida with the theme "The Sun sets on CSICS!!". We're happy to be co-located with the BCTM (same hotel October 19-21), and hope that attendees from both events gain knowledge about the two conferences as they are set to be merged next year.

From CSIC's origins in 1978 as an international gathering for distinguished experts to present their latest results in GaAs IC technology and MMIC design, the symposium has grown to embrace GaN, InP, SiGe, CMOS, and many other emerging technologies. This convergence allows CSICS to offer a perfect blend of state of the art IC performance, innovative design techniques, and advanced device technologies. There are no other events in the world where you can see GaN HPAs, InP THz PAs, Optical CMOS/SiGe transceivers, GaN HEMT power devices, and advances in modeling all presented together.

On Sunday October 22nd, CSICS will offer topical short and primer courses. The first Primer Course will be ***Introduction to MMIC High Power Amplifier Design*** presented by Dr. Chuck Campbell. This primer course serves as an introduction to high power microwave monolithic integrated circuit (MMIC) design. The second Primer Course ***Introduction to Si RF and Mixed Signal IC Design*** will be presented by Prof. Waleed Khalil. This primer provides insight into design of principal RF building blocks, namely PAs, LNAs, mixers and oscillators. The all-day short course will be ***Silicon Photonics Technology and Design*** taught by four industry experts. This course presents an overview of standard and emerging silicon photonic platforms that researchers can access either through multi-project wafer shuttles or arrangements with foundries. Active and passive silicon and hybrid-silicon components, such as polarization management devices, fiber-to-chip couplers, modulators, photodetectors, and lasers, will be reviewed. Combined with BCTM's Short Course offerings on Saturday, October 21st, this rounds out an entire weekend of great learning opportunities.

As a complement to the technical program, the symposium includes numerous social events that allow participants to interact and network in a relaxed setting. These include the Sunday Evening Opening Reception, the Monday Evening Exhibition Reception, and the Technology Exhibition Luncheon on Tuesday. Also on Tuesday, a sunset cruise in the bay behind the hotel on the Biscayne Bay Lady serves as our Theme party. CSICS also offers a daily breakfast and AM/PM coffee breaks on Monday through to Wednesday.

We would like to thank the efforts of the many dedicated volunteers on the CSICS organizing committee and the generous support of the IEEE Electron Devices, MTT, and Solid-State Circuits Societies.

Jim Carroll, Chair
2017 IEEE CSICS

CORPORATE BENEFACTORS

This year, we are pleased to continue with the IEEE Compound Semiconductor IC Symposium Corporate Benefactors Program. This program allows companies interested in compound semiconductors to show their support for the Symposium by making contributions towards the cost of some of our social events.

These additional resources enable the Symposium to increase the quality of our event, as well as allowing companies an opportunity for some tasteful promotional activities. To discuss any of the benefactor opportunities in more depth, please contact:

Jim Carroll
Tel: +1-469-248-5462
E-mail: jim.carroll@ni.com

As of this version, the Corporate Benefactors for the 2017 Compound Semiconductor IC Symposium are as follows.

Gold Level Benefactor

National Instruments

Silver Level Benefactors

Qorvo

Keysight Technologies

OMMIC

Media Partners and Other Partner Conferences

EverythingRF

Microwwaves101.com

Microwaves and RF

Comments regarding the web site or any publicity materials should be directed to the Publicity Chair, Steven Huettner (shuettner@nuvotronics.com). Links to our corporate benefactors appear on our symposium website.

GENERAL INFORMATION

IEEE 39th CSIC Symposium
Oct 22nd - Oct 25th, 2017
Miami Marriott Biscayne Bay
Miami, Florida

REGISTRATION

	Advance (Received by Sept. 23rd)	Regular (After Sept. 23rd or on site)
Symposium Registration		
IEEE Member	$725	$775
Non-IEEE	$775	$875
IEEE Life-Member	$375	$375
Student	$400	$450
One Day - IEEE Member[1]	$360	$440
One Day - IEEE Life Member[1]	$250	$250
One Day - Non-IEEE[1]	$400	$460
One Day - Student[1]	$250	$280
Short/Primer Course		
Short Course	$520	$520
Short Course Student	$270	$270
Primer Course 1+2	$370	$370
Primer Course 1+2 Student	$220	$220
Additional Items		
Guest Opening Cocktail Reception Ticket	$40	$40
Guest Exhibition Opening Reception Ticket	$80	$80
Guest Biscayne Bay Theme Party Ticket	$80	$80
Adtl. Digest USB	$100	$100
Adtl. Short Course USB	$100	$100
Adtl. Primer Course Notes USB	$100	$100
Adtl. Full Access Exhibitor Registration	$300	$300
Adtl. Exhibits Only Registration	$200	$200

All fees are denominated in US$
Full Registration Includes: USB, eBook, all refreshments Monday - Wednesday, continental breakfast Monday - Wednesday, Sunday Reception, Monday Reception, Tuesday Lunch.
Short Course Registration Includes: Short Course Notes on USB, continental breakfast and Short Course Lunch
[1]One-day Registration Includes: USB only (no social functions)
Primer Course Registration includes: Primer Course Notes on USB Only

For **ADVANCE REGISTRATION,** click on the Symposium Registration link on the Symposium website (www.csics.org). Please note that advance registration ends on September 23rd.

For registration and payment related questions, please contact:

IEEE/MCM:
Brianna Hunt, CSICS Registrar,
445 Hoes Lane, Piscataway, NJ, 08854 USA
Tel: +1-844-816-1739
Fax : +1-609-689-0069
Email: csicsreg@ieee.org

The remittance is payable by checks in U.S. dollars only, by personal/company check drawn on a U.S. bank, U.S. currency or traveler's checks. Checks must be made payable to "IEEE/2017 CSICS" and must be encoded with the bank number, account number, and check number. Credit cards may also be used. Bank drafts from non-U.S. banks and foreign currency are unacceptable and will be returned.

When you register for the Conference, the contact information you provide (including your name, address, phone, and email address) may be shared with CSICS and, with your explicit consent, vendor exhibitors.

We urge you to pre-register to reduce your costs and to simplify your check-in at the Symposium. Your Technical Digest and registration materials will be ready for you at the Advance Registration Desk.

Registration Center:

Short & Primer Course Registration only

Sunday, October 22nd	7:00 a.m. – 8:00 a.m.	3rd Floor Foyer

Symposium Registration

Sunday, October 22nd	3:00 p.m. – 8:00 p.m.	3rd Floor Foyer
Monday, October 23rd	7:00 a.m. – 5:00 p.m.	3rd Floor Foyer
Tuesday, October 24th	7:00 a.m. – 5:00 p.m.	3rd Floor Foyer
Wednesday, October 25th	7:00 a.m. – 12:00 p.m.	3rd Floor Foyer

Refund Policy:

All requests for refund/cancellation must be received in writing by September 23rd, 2017. No refunds can be provided after this date. Cancellations will incur a US$50 administration fee. Please submit cancellation requests via email to (csicsreg@ieee.org).

ACCOMMODATIONS

Hotel Reservations:

A block of rooms has been reserved at special discounted rates for Symposium participants at our headquarters hotel, the Miami Marriott Biscayne Bay. The hotel is moments away from countless sites to experience from the Design Districts haute couture shopping to the murals of Wynwood that frame a vibrant path to exploring all that Miami has to offer with outstanding restaurants, shopping and extraordinary entertainment. Located 10 minutes from South Beach and 15 minutes from Miami International Airport, you are conveniently connected and right in the middle of it all.

Hotel Address and Phone Numbers:

Miami Marriott Biscayne Bay
1633 North Bayshore Drive
Miami, Florida 33132
TEL: +1-305-374-3900
http://www.marriott.com/hotels/travel/miabb-miami-marriott-biscayne-bay/

While there are alternatives, we would like to remind attendees to please support the Symposium and fully enjoy all the activities on offer by staying at the official headquarters hotel. The Symposium relies on attendees staying at the conference Hotel to reduce the costs charged for the use of meeting rooms. Room reservations should be made as soon as possible, as there are a limited number available at the symposium rate. To qualify for the discounted rate reservations must be made by 5:00pm Eastern time, September 29, 2017. Rooms are available at the special Symposium group rate of US$179 per night. Wireless internet is $1 per day in sleeping rooms. These rates do not include room taxes, which are 13%.

To make a reservation, you can follow the link on the symposium website or contact the hotel direct at 1-305-374-3900 and ask for Reservations. Be certain to request the Special Group Rate for the IEEE CSIC Symposium or on-line at:

https://aws.passkey.com/event/15933706/owner/2840/home

Rooms will be subject to availability and possibly be charged at higher rates after September 29, 2017. Check-in time is 3 p.m.; check-out time is 12 noon. If necessary, you may cancel your reservation 48 hours prior to arrival to avoid a one (1) night plus tax penalty charge.

TRANSPORTATION

Travel:

Travel arrangements using the IEEE negotiated air carriers or the carriers of your choice can be made through World Travel, Inc. by calling between the hours of 8:00 a.m. and 5:30 p.m. EST Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (+1 800 879 4333); and outside of the US and Canada, call +1 717 556 1100. Or, you may visit their on-line travel service web site at http://www.ieee.org/travel. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere. Alternatively, you can e-mail your request to ieee@worldtravelinc.com.

IEEE corporate car rental discounts are also available to all attendees of the symposium. Discount codes below entitle attendees to receive special rates that have also been negotiated with Avis A606000, Budget X520000, Hertz 61368, and Enterprise NA24IE1.

Airport Transportation:

Two airports serve the Miami area. The Miami International Airport (MIA) is about 9 miles from the Miami Marriott Biscayne Bay Hotel. The Fort Lauderdale International Airport is about 28 miles from the hotel. Both airports accommodate domestic and international travel.

Airport Transfer:

Transfer to and from the airport can be made by means of shuttle or taxi.

From Miami Int'l Airport:
SuperShuttle: Cost: approx. US$20.00 one way per person (subject to change) with pick up outside of baggage claim area.
Taxi: approx. US$35-US$50 one way, depending on traffic and time of day with pick up outside of baggage claim area.
Uber: US18-US$45 one way, depending on traffic and time of day with pick up outside of baggage claim area.

From Fort Lauderdale Int'l Airport:
SuperShuttle: Cost: approx. US$50.00 one way per person (subject to change) with pick up outside of baggage claim area.
Taxi: approx. US$80-US$120 one way, depending on traffic and time of day with pick up outside of baggage claim area.
Uber: US$50-US$100 one way, depending on traffic and time of day with pick up outside of baggage claim area.

Driving Directions:

From Miami Int'l Airport: Take 836 E. to 395 (Miami Beach) Exit. Exit to Biscayne Blvd, turn left onto Biscayne Blvd. Turn right on NE 14th Street. Go 1 block, turn left onto North Bayshore Drive. Hotel is on the right side of street at 1633 N. Bayshore Dr

From Fort Lauderdale Int'l Airport: Take I-95 South to 395 East to Biscayne Blvd exit. Turn left onto Biscayne Blvd. Take a right turn on NE 14th Street. Go one block to N. Bayshore Drive and make a left turn onto N. Bayshore Drive. The hotel is on the right side of street at 1633 North Bayshore Drive.

ADDITIONAL INFORMATION

Distribution of Relevant Information:

The CSIC Symposium will provide an officially designated area near the registration desk to serve as the proper display area for those in need of space to disseminate free material relevant to the CSIC industry. Printed material of any form will not be allowed to be indiscriminately proliferated in the registration area, hallways, lobbies, or other gathering areas, in proximity to the Symposium, technical sessions, evening social activities, panel sessions, or the exhibition.

Photography:

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. No flash photography will be used. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE. Photographs of copyrighted PowerPoint or other slides are for personal use only and are not to be reproduced or distributed. Do not photograph any such images that are labeled as confidential and/or proprietary.

Non Discrimination Policy

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws. For more information on the IEEE policy visit:

http://www.ieee.org/about/corporate/governance/p9-26.html?WT.mc_id=hpf_pol

Breakfast and Lunch Locations:

Breakfasts:

The location of breakfasts will be as follows:

Short Course Registrants (only) –
Sunday, October 22rd Bayview Ballroom

Symposium Registrants –
Monday, October 23rd: Salon F
Tuesday, October 24th: Salon F
Wednesday, October 25th: Salon F

Lunches:

The location of lunches will be as follows:

Short Course Registrants (only) –
Sunday, October 22nd: Bayview Ballroom

Exhibition Luncheon –
Tuesday, October 24th: Salon F

Coffee Breaks:

The location of coffee breaks will be as follows:

Short Course and Primer Course registrants (only) –
Sunday, October 22rd: Salon E

Symposium Registrants –
Monday, October 23th: Salon E
Tuesday, October 24th: Salon E
Wednesday, October 25th: Salon E

Symposium Social Events:

SYMPOSIUM Opening Cocktail

We welcome you to Miami on Sunday evening, October 22nd from 7:00 p.m. to 8:00 p.m. in the Bayview Ballroom of the Miami Marriott Biscayne Bay. Come and meet up with your old friends and make new acquaintances over cheese and wine, beer or soft drinks. One free admission is included with your registration including two drink tickets, and extra reception tickets may be purchased for $40.

EXHIBITION OPENING RECEPTION

The exhibition opening reception will be held on Monday evening, October 23rd from 5:30 p.m. to 7:30 p.m. in the Bayview Ballroom of the Miami Marriott Biscayne Bay. Come along; visit with the exhibitors over light hors d'oeuvres and wine, beer, or soft drinks. One free admission is included with your registration, and extra reception tickets may be purchased for $80.

EXHIBITION BREAKFAST

The Exhibition Breakfast will be hosted on October 24th. Be sure to join us to visit with the exhibitors, ask questions, make deals, and find out what is going on in our industry.

EXHIBITION LUNCHEON

The Exhibition Luncheon will be hosted on October 24th. Be sure to join us to visit with the exhibitors, ask questions, make deals, and find out what is going on in our industry.

THEME PARTY "The Sun Sets on CSICS Cruise"

The CSICS 2017 finale theme party will take place onboard a Miami charter cruise on the "Biscayne Lady Yacht." Attendees will enjoy amazing views of South Florida's emerald waters, celebrity homes and more. All attendees will enjoy luxury, comfort, flavorful menu items and in addition to an experience of a lifetime! Boarding is at 6:00 pm directly at the rear of the Marriott Biscayne Bay. We will return at 10:00 pm sharp! One free admission is included with your registration, and extra theme party tickets may be purchased for $80.

Miami Attractions:

Step into sunshine, where you'll be greeted by the awe-inspiring Magic City with countless sites to experience from the Design District's haute-couture shopping to the murals of Wynwood that frame a vibrant path to exploring all that Miami has to offer with outstanding restaurants, shopping and extraordinary entertainment. Here at the bridge to everything Miami, our waterfront location means more than just breathtaking views – you are at the intersection of the Art and Design districts, which means your stay is surrounded by the incredible, both outside and in.

http://www.marriott.com/hotels/local-things-to-do/miabb-miami-marriott-biscayne-bay/

Miami Weather:

October in Miami brings an average high between 85 and 88°F (29 to 31°C). The minimum temperature usually falls between 72 and 75°F (22 to 24 °C).

SYMPOSIUM HIGHLIGHTS

The technical program for the 2017 IEEE CSIC Symposium consists of 59 technical papers, two panel sessions, an industry exhibit, and one full day short course: “Silicon Photonics Technology and Design.” We are proud to offer two primer level classes, and “Introduction to MMIC High Power Amplifier Design” and “Introduction to Si RFIC and Mixed Signal IC Design”. The “Introduction to MMIC High Power Amplifier Design” class is a new offering for 2017.

This year we have invited 23 papers on a wide range of important topics encompassing advanced device engineering to circuit application using compound and other related semiconductor technologies.

Exciting new developments from a variety of compound semiconductor disciplines will be presented. This year shows considerable interest in a wide variety of GaN HEMT circuits including PAs, LNAs, switches, and high speed track-and-hold circuits. GaN HEMT device advances, device modeling, and high power device thermal management are also covered. The areas of mm-wave and THz circuits are strongly represented across applications such as space exploration, THz communications, and mm-wave 5G applications. InP HBT, CMOS and BiCMOS processes for > 100GHz applications are also presented. Advances in silicon photonics, high data rate serial links, and high-performance digital communications circuits are also reported. Papers will be presented on HBT characterization and modeling, gallium oxide process technology, and Ge/III-V MOSFETs/TFET devices on a Si CMOS platform. As always, there is a tremendous amount of activity in both commercial wireless communications and military electronics.

Late-Breaking News Papers:

We have 10 late breaking new papers in Sessions O and P starting at 1:30PM on Wednesday October 25.

Technical Digest:

Extra USB Technical Digests can be purchased by Symposium registrants through Advance Registration. A limited number of Digests USBs may also be available for sale at the Registration Desk. The cost of the USB ordered through Advance Registration or purchased on-site is $100.

Outstanding Paper Award:

The 2017 IEEE CSIC Symposium will select a contributed paper for the Outstanding Paper Award. All contributed regular papers (not the invited papers) will automatically be considered as candidates. Symposium attendees will have an opportunity to provide feedback through a Symposium questionnaire as well as to the session chairpersons. The award winner will be announced after this year's Symposium with the award being formally presented after the 2017 CSIC Symposium.

Student Paper Competition:

In recognition of the exceptional contributions made by students, CSICS is proud to hold its second annual Student Paper Competition. To participate in the competition, an eligible student must submit a regular contributed paper naming, at a minimum, themselves and their principal supervisor as authors. The Student Paper Finalists must present their own papers at their assigned symposium session. We congratulate our seven Student Paper Finalists for 2017 CSICS. The winner of the student paper competition will be announced at the beginning of Session P at this year's symposium.

Short Course (full day): "Silicon Photonics Technology and Design"

This course presents an introduction to silicon photonics by four experts in the field. The course starts with a discussion of the technology fundamentals (integration approach) and provides demonstrator examples. The second part of the course discusses foundry offerings and the components that are available to designers. The third part of the course discusses the evolutionary trends of this technology and discusses the fundamentals, tools, and applications of this technology. Packaging and integration will also be discussed. Finally, the course concludes with a section on circuit design with a special emphasis on low-noise amplifiers and Mach-Zehnder modulator drivers.

Panel Sessions:

This year we have two exciting Panel Sessions on Monday October 23rd and Tuesday October 24th. These are intended to be timely, thought-provoking, educational, and hopefully controversial. The two panel session topics are:

PANEL SESSION 1:
Optics Invading Copper? The Future of Backplane Communication
Monday, October 23th, 3:30 p.m. - 5:00 p.m.

PANEL SESSION 2:
Have North America and Europe handed the Semiconductor Industry to Asia?
Tuesday, October 24th, 3:30 p.m. - 5:00 p.m.

Please see the "Symposium Program" section later in this brochure for more complete descriptions of each of these Panel Sessions (listed according to day and time).

Technology Exhibition

The 2017 IEEE CSICS Technology Exhibition will be held on Monday evening October 23th and Tuesday the 24th in the **Salon F** and is open to all Symposium registrants. The combined exhibition gives companies and attendees access to the entire array of compound semiconductor products and services, i.e., materials, manufacturing, device technology, integrated circuits, as well as the latest information on modeling and design simulation tools. This year's exhibitors are:

Hi-Solar Co., Ltd.
Keysight Technologies
Maury Microwave Corp.
Microsanj, LLC
Modelithics, Inc.
NI-AWR Group
Presidio Components, Inc.
Silvaco
Sonnet Software, Inc.
StratEdge Corp.
Wolfspeed (formerly Cree)

The Exhibition will feature informative and interesting displays with corporate representatives on hand between the hours of 5:30 p.m. and 7:30 p.m. on Monday, October 23rd, and between 7:30 a.m. and 3:30 p.m. on Tuesday, October 24th. The Exhibition will also host the Exhibition Opening Reception from 5:30 p.m. until 7:30 p.m. on Monday evening and the Exhibition Luncheon from 12:00 noon to 1:30 p.m. on Tuesday. The Exhibition Opening Reception, the Exhibition Luncheon, and the Tuesday coffee breaks will be held in the exhibition area in the **Salon F**.

To participate in the Exhibition, please contact Candi Wooldridge (MP Associates), candi@mpassociates.com, (303) 530-4562. Please visit the Symposium website at www.csics.org for additional information.

Short Course

Sunday, October 22nd, 2017
Miami Marriott Biscayne Bay - Watson
8:00a.m. – 5:25p.m.

Course Coordinator: **Pete Zampardi**
Qorvo
(805) 480-5087
Pete.Zampardi@Qorvo.com

CSICS 2017 Short Course and Schedule

Silicon Photonics Technology and Design

Date: Sunday, October 22, 2017
Time: 8:00am - 5:25pm
Location: Room Watson
Session Chair: Pete Zampardi (Qorvo)
Co-Chair: Patrice Gamand, XLIM Laboratory University of Limoges

7:00 - 8:00 AM **Registration and breakfast**

8:00 - 8:05 AM **Welcome**

Course Overview

This course presents an introduction to silicon photonics by four experts in the field. The course starts with a discussion of the technology fundamentals (integration approach) and provides demonstrator examples. The second part of the course discusses foundry offerings and the components that are available to designers. The third part of the course discusses the evolutionary trends of this technology and discusses the fundamentals, tools, and applications of this technology. Packaging and integration will also be discussed. Finally, the course concludes with a section on circuit design with a special emphasis on low-noise amplifiers and Mach-Zehnder modulator drivers.

8:05 - 9:55 AM

Monolithic Photonic BiCMOS Technology: Enabler for High-Speed Transceiver Applications

Instructor: Stefan Lischke (IHP Microelectronics)

Photonic-electronic integration is a key technology to master data traffic growth and therefore an enabler of future network technologies. For some time now, a novel silicon-based photonic-electronic integration technology, photonic BiCMOS, is under development at IHP. Photonic BiCMOS is a planar technology co-integrating monolithically on a single substrate high-speed RF frontend electronics with high-speed photonic devices such as broadband germanium detectors, modulators, and SOI

nano-waveguide integrated optics. High RF capability of this electronic photonic integrated circuit (ePIC) technology is enabled by SiGe heterojunction bipolar transistors (HBTs), which are integrated with 0.25µm CMOS. This talk reviews the integration approach deployed in the photonic BiCMOS and discusses performance issues for both, electronic and photonic devices. Measures to overcome detrimental integration effects will be discussed. Examples of transmitter and receiver demonstrators are presented to indicate the potential for monolithically integrated high-speed transceivers at 1550 nm.

Stephan Lischke received the B.Sc. and M.Sc. degrees in Physics with specialization in Semiconductor Technology from the Technical University Brandenburg, Cottbus in 2005 and 2007, respectively. He is currently a Researcher in the Silicon Photonics group within the Technology department of IHP, Frankfurt (Oder), Germany. His current work is focused on Germanium photo detectors and the integration of photonic devices into IHP's photonic BiCMOS process.

9:55 - 10:25 AM Break

10:25 AM - 12:15 PM

Introduction to Silicon Photonics: Foundry-Manufactured Platforms and Devices

Instructor: Joyce Poon (University of Toronto)

This talk presents an overview of the standard and emerging silicon photonic platforms that researchers or designers can access either through multi-project wafer shuttles or arrangements with foundries. Standard platforms only have one waveguide layer in silicon, while emerging platforms can incorporate several waveguide layers and hybrid III-V integration. Active and passive silicon and hybrid-silicon components, such as polarization management devices, fiber-to-chip couplers, modulators, photodetectors, and lasers, will be reviewed.

Joyce Poon is a Professor of Electrical and Computer Engineering at University of Toronto, where she holds the Canada Research Chair in Integrated Photonic Devices. She and her team conduct theoretical and experimental research in micro- and nano-scale integrated photonics. Dr. Poon obtained the Ph.D. and M.S. in Electrical Engineering from Caltech in 2007 and 2003 respectively, and the B.A.Sc. in Engineering Science (physics option) from the University of Toronto in 2002.

12:15 - 1:15 PM Lunch

1:15 - 3:05 PM

Silicon Photonics Technology and Impact on Designs

Instructor: Christophe Kopp (CEA-LETI)

Silicon photonics technology has definitely reached a first level of maturity with several industrial products and available fabrication supply chains. Thanks to current innovations with heterogeneous material integration and multi photonic layer stacking, the next generation will represent a new paradigm for designers to address a wider field of applications beyond optical communications. This short course discusses both fundamentals, tools and applications of silicon photonics. We will

go through the evolution and the current trend of technologies of silicon photonics. We will review the device library dedicated to build photonic integrated circuits for high speed optical communications. We will also describe the developments in packaging and integration to build devices for fiber optic network to many-core processor architectures.

Dr. Christophe Kopp received the Ph.D. degree in photonic engineering from the University of Strasbourg, Alsace, France, in 2000, in the field of diffractive optics. Since 2001, he has been with the LETI (CEA TECH) Institute, Grenoble, France, where he is engaged in developing micro-optoelectronic devices. He has participated in national and European collaborative projects (ODIN, HELIOS, WADIMOS MICROS, SILVER, PLAT4M, IRIS). In connection with industrial companies (Intexys Photonics, IIIV-lab Mapper lithography, STm), he has been responsible for R&D projects. He is the author or co-author of more than 70 papers in scientific journals and international conference proceedings, one scientific book, and more than 30 patents. Currently, he is at the head of the laboratory of silicon photonics with 35 research engineers/technicians and 6 PhD students.

3:05 - 3:25 PM Break

3:25 - 5:15 PM

Circuit Design for Si Photonics

Instructors: Peter Schvan (Ciena)

The use of Si Photonics promises economical implementation of large volume low cost E-O modules for various optical communication applications. These solutions need to support high bit rate, currently up to 400 Gb/s, and low power dissipation. Beside the implementation of the necessary optical devices the design of the required electrical components also poses significant challenges. These include the connection between electronics and optics, compensation for some of the limitations of Si based optical components particularly for modulators, achieving low crosstalk penalty and also the requirement to fit them into a very low power budget. This course will review circuit solutions to design low noise amplifiers and MZ modulator drivers for SiP based receiver and transmitter systems.

Peter Schvan received his M.S. in Physics and his Ph. D. in Electronics in 1985. After joining Nortel he has worked in the area of device modeling, CMOS and BiCMOS technology development followed by circuit design for fiber optic and wireless communication using SiGe, BiCMOS, InP and CMOS technologies. Currently he is director of analog design at Ciena, Ottawa, involved in the development of broadband amplifiers, high speed A/D and D/A converters. He gave several workshop presentations and authored or co-authored over 40 publications.

5:15 - 5:25 PM Course Evaluation

Short Course Schedule

The short courses will be held on Sunday October 22rd in Watson. A continental breakfast is available to all registered Short Course attendees and instructors. The short course, “Silicon Photonics Technology and Design”, will begin at 8:00 am and finish at 5:25 pm. A lunch will be provided as well as morning breakfast at 7am and afternoon refreshment break.

Who Should Attend

The first course is intended to appeal to both technologists and circuit designers of all backgrounds who have an interest in understanding the Silicon Photonics Technology and Design. . This course presents an introduction to silicon photonics by four experts in the field. The course starts with a discussion of the technology fundamentals (integration approach) and provides demonstrator examples. The second part of the course discusses foundry offerings and the components that are available to designers. The third part of the course discusses the evolutionary trends of this technology and discusses the fundamentals, tools, and applications of this technology. Packaging and integration will also be discussed. Finally, the course concludes with a section on circuit design with a special emphasis on low-noise amplifiers and Mach-Zehnder modulator drivers.

Short Course Pre-Registration

So that we may properly plan for attendance, we encourage you to pre-register for the Short Courses. The registration fee for the full-day Short Course is $520 for professionals and $270 for students. This includes attending the lectures, notes for both Short Courses available for download and on a USB stick, a continental breakfast, a lunch and morning/afternoon refreshments during breaks. Additional copies of the Short Course Notes on USB may be purchased for $100 each.

Primer Courses

Sunday, October 22rd in Hibiscus
8:00 a.m. – 7:00 p.m.

Primer Course Coordinator: **Thé Linh Nguyen**
Finisar Corporation
Sunnyvale, CA
thelinh.nguyen@finisar.com

Primer Course 1 - Introduction to MMIC High Power Amplifier Design

Instructor: Charles F. Campbell
Qorvo
Richardson, TX

Course Objective and Description:

This primer course was developed to serve as an introductory level course on high power microwave monolithic integrated circuit (MMIC) amplifier design. Covered material will start with reactively matched power amplifiers and conclude with wideband power amplifier design. Circuit topologies will be presented, analyzed and transformed into a monolithically compatible form. Various aspects and limitations of transistor and MMIC technology are highlighted as the circuit functions are developed. Where available fabricated examples of Galium Nitride (GaN) power amplifier MMICs will be presented.

Primer Agenda:

8:00 AM **Introduction and Overview**

Reactively Matched Power Amplifier Design

- Power Amplifier Specifications
- Transistor Cell Selection
- Matching Network Synthesis
- Stability Analysis

Wideband Power Amplifier Design

- Bandwidth Limitations
- Wideband Topologies
- Circuit Design
- Biasing and Transformers
- MMIC Examples

9:30 AM **Coffee Break**

Primer Course 2 - Introduction to Si RFIC and Mixed Signal IC Design

Instructor: Prof. Waleed Khalil
The Ohio State University
Columbus, OH

Course Objective and Description:

CMOS technology is the predominant technology for RF and mixed signal ICs owing to its low cost, ease of integration with digital functions, and increasing speed/performance. This course is intended for semiconductor professionals of all technical backgrounds who wish to learn or refresh their understanding of the fundamentals of S device and circuits technology. The primer will begin with an overview of the nanoscale CMOS transistors and integrated passives from a device/technology perspective, analyzing key concepts in device modeling. This will be followed by a brief comparison to SiGe BJT device technology illustrating key differences. In so doing, the intent is to provide guidance on how the circuit design process differs and to enlighten attendees on subjects such as transistor sizing and biasing practices. In the second part of the primer, the focus will shift to the key building blocks that make up Silicon based integrated transceivers. Among the blocks to be covered in the RF domain are: LNAs, Mixers and VCOs and in the mixed signal domain are: GHz Track and Hold circuits, amplifiers and DACs. For each one, designers are confronted with a variety of different circuit topologies, each with its attendant strengths and performance metrics. Making the right choice very much depends on having an awareness of what the options are, good specmanship and how to optimize to get the best performance.

The course instructor, Dr. Waleed Khalil, is currently serving as an Associate professor at the ECE department and the ElectroScience Lab, The Ohio State University. Prior to joining Ohio State, Prof. Khalil spent 16 years at Intel Corporation where he held various technical and leadership positions in wireless and wireline communication groups. While at Intel, he established Intel's first analog device modeling methodology for mixed signal circuit design and also contributed to the development of Intel's first RF process technology. Prof. Khalil's current research spans CMOS, SiGe and III-V technologies with focus on RF and mm-wave circuits and systems, high performance clocking circuits, GHz D/A and D/H circuits..

Primer Agenda:

10:00 AM **Introduction and Overview of Course Objectives**

10:10 AM **CMOS Technology Perspective: A Device Modeling Discussion**

12:00 PM **Lunch**

1:15 PM **Brief Introduction to SiGe HBT Technology and Comparison with CMOS**

1:45 PM **RF CMOS Block Level Design Fundamentals and Examples**

4:00 PM **Coffee Break**

4:30 PM **Mixed Signal Block Level Design Fundamentals and Example**

7:00 PM Close of Primer 2

Student Paper Finalists

Competition Chair: Prof. Waleed Khalil
The Ohio State University
Columbus, OH

Presentation Schedule for the seven Student Paper Finalists:

Tuesday, October 24, 9:30 a.m (Salon E)

D.3 **An AC Coupled 10 Gb/s LVDS-compatible Receiver with Latched Data Biasing in 130 nm SiGe BiCMOS**
B. Mathieu[1,2], J. J. McCue[3], B. Dupaix[1], V. J. Patel[2], S. Dooley[2], H. Lavasani[4], J. Wilson[5], and Waleed Khalil[1], *[1]ElectroScience Laboratory, The Ohio State University, Columbus, USA, [2]Air Force Research Laboratory, Dayton, USA, [3]The Knowledge Design Company, Dayton, USA, [4]Qualcomm Inc., San Diego, USA, [5]Army Research Laboratory, Adelphi, USA*

Tuesday, October 24, 11:00 a.m. (Salon ABCD)

G.2 **Innovative Submicron Thermal Characterization Method for AlGaN/GaN Power HEMTs with Hyperspectral Thermoreflectance Imaging**
G. Brocero[1,2], D. Kendig[3], A. Shakouri[4], Y. Guhel[1], Ph. Eudeline[2], J-P Sipma[2] and B. Boudart[1], *[1]Groupe de Recherche en Informatique, Image, Automatique et Instrumentation de Caen Normandie Universite, Caen, France, [2]Thales Air Systems SAS, Ymare, France, [3]Microsanj LLC, Santa Clara, USA, [4]Purdue University, West Lafayette, USA.*

Tuesday, October 24, 11:20 a.m. (Salon ABCD)

G.3 **Electro-Thermal Characterization of GaN HEMT on Si through Self-Consistent Energy Balance-Cellular Monte-Carlo Device Simulations**
A. Latorre-Rey[1], K. Merrill[1], J. Albrecht[2] and M. Saraniti[1], *[1]Arizona State University, Tempe, USA, [2]Michigan State University, East Lansing, USA*

Wednesday, October 25, 9:00 a.m. (Salon ABCD)

K.2 **InAlN/GaN HEMT Using Microwave Annealing for Low Temperature Ohmic Contact Formation**
L. Chou[1], L. Peng[1], H.C. Wang[1], H. Chiu[1], H.T. Wang[1], D. Chiang[1], J. Chyi[2], *[1]Chang Gung University, Taoyuan City, Taiwan, [2]National Central University, Taoyuan City, Taiwan*

Wednesday, October 25, 9:30 a.m (Salon E).

J.3 **Balanced Active Frequency Multipliers in D and G bands Using 250nm InP DHBT Technology**
S. Carpenter, Z. S. He, and H. Zirath,
Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Goteborg, Sweden

Wednesday, October 25, 11:00 a.m. (Salon E).

L.2 **A 5-15 GHz Stacked I/Q Modulator with 15-19 dBm OP1dB and 26-30 dBm OIP3 in 45 nm SOI CMOS**
S. Zihir and G. Rebeiz , *University of California San Diego, La Jolla, USA*

Wednesday, October 25, 11:20 a.m. (Salon E).

L.3 **Fully Differential High Input Power Handling Ultra-Wideband Low Noise Amplifier for MIMO Radar Application**

M. Sakalas[1], P. Sakalas[2, 3], N. Joram[1], F. Ellinger[1], *[1]Chair for Circuit Design and Network Theory, Technische Universitat Dresden, Germany, [2]Chair for Electronic Devices and Integrated Circuits, Technische Universitat Dresden, Germany, [3]Fluctuation Research Laboratory, Center of Physical Sciences and Technologies, Vilnius, Lithuania*

CSIC Symposium Opening Cocktail Hour

Bayview Ballroom
Sunday October 22nd
7:00 p.m. - 8:00 p.m.

Monday, October 23th, 2017

SYMPOSIUM PROGRAM

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – 3rd Floor Foyer

7:00 a.m. – 8:15 a.m.
Continental Breakfast – Salon F

SYMPOSIUM OPENING

8:15 a.m. – 8:45 a.m.
Salon E – Miami Marriott Biscayne Bay

Opening Remarks
2017 Symposium General Chair
Jim Carroll, NI – AWR Group

Technical Program Overview
2017 Technical Program Chair
Brian Moser, Qorvo

SESSION A: Plenary Session

8:45 a.m. – 12:00 p.m.
Salon E– Miami Marriott Biscayne Bay

Chairpersons: Peter Zampardi, *Qorvo*
Bruce Green, *NXP Semiconductors.*

8:45 a.m.
A.1 **Hybrid CMOS System-on-Chip/InP MMIC Systems for Deep-Space Planetary Exploration at mm-Wave and THz (Invited)**
A. Tang[1,2], Theodore Reck[1,2], [1]*Jet Propulsion Laboratory, California Institute of Technology, Pasadena, United States,* [2]*University of California, Los Angeles, United States*

9:15 a.m.
A.2 **Technology Options for mm-wave Test and Measurement Equipment (Invited)**
D. DiSanto, T. Shirley, and R. Shimon, *Keysight Technologies, Santa Rosa,, United States*

9:45 a.m.
A.3 **Nanostructured GaN Transistors (Invited)**
N. Chowdhury, T. Palacios**,** *Massachusetts Institute of Technology, Cambridge, USA*

10:15 a.m. – 10:30 a.m.
Coffee Break

Monday, October 23th, 2017

10:30 a.m.
A.4 **Design of Monolithic Silicon Photonics at 25 Gb/s (Invited)**
J. S. Orcutt, *IBM Research, Yorktown Heights, United States*

11:00 a.m.
A.5 **UHF Power Conversion with GaN HEMT Class-E2 Topologies (Invited)**
J. A. García, M. Nieves Ruiz, and D. Vegas, *University of Cantabria, Spain*

11:30 a.m.
A.6 **GaN Non-Uniform Distributed Power Amplifier MMICs – The Highs and Lows (Invited)**
C. F. Campbell, *Qorvo, Richardson, United State*

12:00 p.m.
End of Session A

12:00 p.m. – 1:30 p.m.
Break for Lunch

Monday, October 23th, 2017

SESSION B: GaN-Based Systems and Components

1:30 p.m. – 3:00 p.m.
Salon E – Miami Marriott Biscayne Bay Hotel

Chairpersons: Michael Roberg, *Qorvo*
Simon Wood, *Wolfspeed*

1:30 p.m.
B.1 **Next Generation Radar (Invited)**
A. Darwish, K. McKnight, J. Penn, E. Viveiros, A. Hedden, and A. Hung, *Army Research Laboratory, Adelphi, USA*

2:00 p.m.
B.2 **Packaged 7 GHz GaN MMIC Doherty Power Amplifier**
D. Gustafsson, A. Leidenhed, and K. Andersson, *Ericsson AG, Gothenburg, Sweden*

2:20 p.m.
B.3 **Wideband High Power SPDT and SP3T GaN MMIC Switches in Low-Cost Overmolded Plastic Package**
T. Nguyen, V. Zomorrodian, and T. Kywe, *Qorvo, Richardson, USA*

2:40 p.m.
B.4 **A Reconfigurable C-/X-band GaN Cascode LNA MMIC**
K. Kobayashi[1], C. Campbell[1], C. Lee[1], J. Gallagher[2], J. Shust[2], and A. Botelho[2], *[1]Qorvo – IDP Research, Richardson, USA, [2]Lockheed Martin – Rotary & Mission Systems, Moorestown, USA*

3:00 p.m.
End of Session B

3:00 p.m. – 3:30 p.m.
Coffee Break

SESSION C: Characterization and Analysis of HBTs

1:30 p.m. – 3:00 p.m.
Salon ABCD – Miami Marriott Biscayne Bay

Chairpersons: Michael Schröter, *TU Dresden, Germany / UC San Diego, CA, USA*
Subrata Halder, *Qorvo, Greensboro, USA*

1:30 p.m.
C.1 **IC calibration kits and de-embedding techniques for sub-mm-wave device characterization (Invited)**
M. Spirito, I. Galatro, *TU Delft, Delft, Netherlands*

2:00 p.m.
C.2 **Harmonic distortion analysis of InP HBTs with 650 GHz f_{max} for high data rate communication systems**
P. Sakalas[1,2], M. Schröter[1,3], T. Nardmann[1], H. Zirath[4], *[1]TU Dresden, [2]FRL, Vilnius, Lithuania , [3]UC San Diego, La Jolla, CA, USA, [4]Chalmers University, Göteborg, Sweden*

2:20 p.m.
C.3 **Characteristics of substrate-induced low-frequency oscillations in GaAs devices and circuits**
M. Iwamoto, C. Hutchinson, B. Luk, T. Low, D. D'Avanzo, *Keysight Technologies, Santa Rosa, USA*

2:40 p.m.
C.4 **Numerical analysis of the thermal behavior sensitivity to technology parameters and operating conditions in InGaP/GaAs HBTs**
A. Catalano[1], A. Magnani[1], V. d'Alessando[1], L Codecasa[2], N. Rinaldi[1], B. Moser[3], P. Zampardi[3], *[1]Univ. Frederico II, Naples, Italy, [2]Politecnico di Milano, Milan, Italy, [3]Qorvo, Newbury Park, USA*

3:00 p.m.
End of Session C

3:00 p.m. – 3:30 p.m.
Coffee Break

Monday, October 23th, 2017

PANEL SESSION 1: Optics Invading Copper? The Future of Backplane Communication

3:30 p.m. – 5:00 p.m.
Salon E – Miami Marriott Biscayne Bay

Organizer: Thomas Toifl, *IBM Zurich Research Laboratory*

Moderator: Shahriar Shahramian, *Nokia - Bell Labs*

This panel will discuss the future of backplane communication. The familiar electrical links offer low cost and simple packaging, however the demand on backplane data rates appear to exceed the improved material and advanced coding schemes. The shrinking link margins may push designers to consider optical backplane communication as data rates invade fiber-like speeds. Considering that advancements to data-converters is medium-agnostic, is the future of backplane links bright? Our panel members will discuss the trade-offs between electrical and optical backplane solutions and offer their vision of the future.

Panel Members:

Tod Dickson	*IBM*
Clint Schow	*University of California Santa Barbara*
Ali Sheikholeslami	*University of Toronto*
Brian Welch	*Luxtera*

5:00 p.m.
End of Panel Session 1

Technology Exhibition
Opening Reception
Salon F
5:30 p.m. - 7:30 p.m.

Tuesday, October 24th, 2017

REGISTRATION, EXHIBITION, AND BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – 3rd Floor Foyer

7:30 a.m. – 3:30 a.m.
Technology Exhibition – Salon F

7:30 a.m. – 8:30 a.m.
Exhibition Breakfast – Salon F

SESSION D: High Speed Serial Links

8:30 a.m. – 9:50 a.m.
Salon E – Miami Marriott Biscayne Bay

Chairpersons: Thé Linh Nguyen, *Finisar.*
Shahriar Shahramian, *Nokia - Bell Labs.*

8:30 a.m.
D.1 **Design Techniques for 32.75Gb/s and 56Gb/s Wireline Transceivers in 16nm FinFET (Invited)**
D. Turker, P. Upadhyaya, J. Im, S. Chen, Y. Frans, K. Chang, *Xilinx, Inc., San Jose, USA*

9:00 a.m.
D.2 **ADC Based Clock Recovery for Serial Links (Invited)**
A. Sheikholeslami, *University of Toronto, Toronto, Canada*

9:30 a.m.
D.3 **An AC Coupled 10 Gb/s LVDS-compatible Receiver with Latched Data Biasing in 130 nm SiGe BiCMOS**
B. Mathieu[1,2], J. J. McCue[3], B. Dupaix[1], V. J. Patel[2], S. Dooley[2], H. Lavasani[4], J. Wilson[5], and Waleed Khalil[1], *[1]ElectroScience Laboratory, The Ohio State University, Columbus, USA, [2]Air Force Research Laboratory, Dayton, USA, [3]The Knowledge Design Company, Dayton, USA, [4]Qualcomm Inc., San Diego, USA, [5]Army Research Laboratory, Adelphi, USA*

9:50 a.m.
End of Session D

10:00 a.m. – 10:30 a.m.
Coffee Break

Tuesday, October 24th, 2017

SESSION E: Advanced Devices and Modeling

8:30 a.m. – 9:50 a.m.
Salon ABCD – Miami Marriott Biscayne Bay

Chairpersons: Sansaptak Dasgupta, *Intel Corp.*
Bruce Green, *NXP Semiconductors*

8:30 a.m.
E.1 **Ultra-low Lower MOSFET and Tunneling FET Technologies Using III-V and Ge (Invited)**
S. Takagi and M. Takenaka, *Dept. of Electrical Engineering and Information Systems, The University of Tokyo, Tokyo, Japan*

9:00 a.m.
E.2 **The Interplay of Thermal, Time and Poole-Frenkel Emission on the Trap-based Physical Modeling of GaN HEMT Drain Characteristics**
C. Chen, R. Sadler, D. Wang, D. Hou, Y. Yang, W. Yau, S. Wang, M. Wu, T. Wu, R. Chen, and B. Ou, *GCS, Torrance, USA*

9:20 a.m.
E.3 **Raytheon High Power Density GaN Technology (Invited)**
R. Leoni, N. Kolias, P. Jablonski, F. Altunkilic, E. Johnson, and W. Bourcy, *Raytheon Integrated Defense Systems, Andover, United States*

9:50 a.m.
End of Session E

10:00 a.m. – 10:30 a.m.
Coffee Break

Tuesday, October 24th, 2017

SESSION F: Advancements of mm-Wave & THz Circuits in Silicon

10:30 a.m. – 11:40 a.m.
Salon E – Miami Marriot Biscayne Bay

Chairpersons: Shahriar Shahramian, *Nokia - Bell Labs*
Bryan Wu, *Northrop Grumman*

10:30 a.m.
F.1 **Layout optimizations for THz Integrated Circuit design in bulk nanometer CMOS (Invited)**
W. Steyaert, Patrick Reynaert,
ESAT-MICAS, KU Leuven, Leuven, Belgium

11:00 a.m.
F.2 **A Fully Decoupled LC Tank VCO based 16 to 19 GHz PLL in 130nm SiGe BiCMOS Achieving -131dBc/Hz Phase Noise at 10MHz Offset**
B. Sadhu, S.K. Reynolds,
IBM T. J. Watson Research Center, Yorktown Heights, USA

11:20 a.m.
F.3 **A Fully-Integrated 94-GHz 16-Element Dual-Output Phased-Array Transmitter in SiGe BiCMOS with PSAT>6.5 dBm up to 105 C**
W. Lee[1], C. Ozdag[2], Y. Aydogan[3], J-O, Plouchart[1], M. Yeck[1], A. Cabuk[2], A. Kepkep[2], E. Apaydin[2], A. Valdes-Garcia[1],
[1]IBM T. J. Watson Research Center, Yorktown Heights, USA,
[2]MKR-IC, Istanbul, Turkey,
[3]Aselsan Inc., Ankara, Turkey

11:40 a.m.
End of Session F

SESSION G: GaN Devices are Muy Caliente: Thermal Characterization of GaN HEMTs

10:30 a.m. – 11:40 a.m.
Salon ABCD – Miami Marriott Biscayne Bay

Chairpersons: Robert Howell, *Northrop Grumman Corp.*
Akio Wakejima, *Nagoya Institute of Technology.*

10:30 a.m.
G.1 **Transient Thermoreflectance Wafer Mapping for Process Control and Development: GaN-on-Diamond (Invited)**
J. Pomeroy, R. Simon, C. Middleton and M. Kuball, *University of Bristol, Bristol, United Kingdom*

11:00 a.m.
G.2 **Innovative Submicron Thermal Characterization Method for AlGaN/GaN Power HEMTs with Hyperspectral Thermoreflectance Imaging**
G. Brocero[1,2], D. Kendig[3], A. Shakouri[4], Y. Guhel[1], Ph. Eudeline[2], J-P Sipma[2] and B. Boudart[1], *[1]Groupe de Recherche en Informatique, Image, Automatique et Instrumentation de Caen Normandie Universite, Caen, France, [2]Thales Air Systems SAS, Ymare, France, [3]Microsanj LLC, Santa Clara, USA, [4]Purdue University, West Lafayette, USA.*

11:20 a.m.
G.3 **Electro-Thermal Characterization of GaN HEMT on Si through Self-Consistent Energy Balance-Cellular Monte-Carlo Device Simulations**
A. Latorre-Rey[1], K. Merrill[1], J. Albrecht[2] and M. Saraniti[1], *[1]Arizona State University, Tempe, USA, [2]Michigan State University, East Lansing, USA*

11:40 a.m.
End of Session G

Technology Exhibition Lunch
Salon F
12:00 p.m. – 1:30 p.m.

SESSION H: III/V Solutions for 5G Applications

1:30 p.m. – 3:00 p.m.
Salon E – Miami Marriot Biscayne Bay

Chairpersons: Kazuya Yamamoto, *Mitsubishi Electric Corp.*
Marc Rocci, *OMMIC SAS*

1:30 p.m.
H.1 **3D/Inkjet-Printed Millimeter Wave Components and Interconnects for Communication and Sensing (Invited)**
A. Georgiadis[1], J. Kimionis[2], M. Tentzeris[2], Heriot-Watt[1]
[1]University, Edinburgh, Edinburgh, UK,
[2]Georgia Institute of Technology, Atlanta, USA

2:00 p.m.
H.2 **10-W Power Amplifier and 3-W Transmit/Receive Module with 2.7-dB NF in Ka-Band Using a 100-nm GaN/Si Process**
A. Gasmi, M. Kaamouchi, J. Poulain, F. Lecourt, G. Dagher, P. Frijlink, and R. Leblanc,
OMMIC SAS, Limeil Brevannes, France

2:20 p.m.
H.3 **A CW 20-W Ka-Band GaN High Power MMIC Amplifier with a Gate Pitch Designed by Using One-Finger Large-Signal Models**
Y. Yamaguchi, J. Kamioka, M. Hangai, S. Shinjo, and K. Yamanaka,
Mitsubishi Electric Corporation, Kamakura, Japan

2:40 p.m.
H.4 **Scalable Vanadium Dioxide Switches with Sub-Millimeter Wave Bandwidth**
C. Hillman, P. Stupar, and Z. Griffith,
Teledyne Scientific & Imaging, Thousand Oaks, USA

3:00 p.m.
End of Session H

Tuesday, October 24th, 2017

SESSION I: GaN HEMT Modeling for Amplifier Design

1:30 p.m. – 2:40 p.m.
Salon ABCD – Miami Marriott Biscayne Bay

Chairpersons: Masaya Iwamoto, *Keysight Technologies*
Peter Zampardi, *Qorvo.*

1:30 p.m.
I.1 **Artificial Neural Networks for Compound Semiconductor Device Modeling and Characterization (Invited)**
J. Xu and D. Root, *Keysight Technologies, Santa Rosa, USA*

2:00 p.m.
I.2 **HEMT Model with Internal Nodes Access and Custom CDS Function for Amplifier Design**
F. Kharabi, *Qorvo, Greensboro, USA.*

2:20 p.m.
I.3 **GaN Device-Circuit Interaction on RF Linear Power Amplifier Designed using MVSG Compact Model**
P. Choi, U. Radhakrishna, D. Antoniadis and E. Fitzgerald, *Massachusetts Institute of Technology, Cambridge, USA*

2:40 p.m.
End of Session I

Tuesday, October 24th, 2017

PANEL SESSION 2: Have North America and Europe handed the Semiconductor Industry to Asia?

3:30 p.m. – 5:00 p.m.
Salon E – Miami Marriott Biscayne Bay

Moderators: Shahriar Shahramian, *Nokia – Bell Labs*

The development of next generation CMOS technology nodes has been heavily focused in Asia primarily due to the inexorable rise of foundry infrastructure and operation costs. As a result, the majority of fabless semiconductor industries rely solely on a handful of foundries for their product manufacturing and development. Simultaneously, competing fabless Asian companies demand a larger share of the foundry throughput. Do North America and Europe stand the risk of losing the semiconductor industry, and by proxy the entire communication industry, to Asia?

Panel Members:

Pascal Chevalier	*STMicroelectronics*
Vadim Issakov	*Infineon*
Ed Preisler	*TowerJazz*

5:00 p.m.
End of Panel Session 2

Wednesday, October 25th, 2017

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – 3rd Floor Foyer

7:00 a.m. – 8:30 a.m.
Continental Breakfast – Salon F

SESSION J: THz Systems and Applications

8:30 a.m. – 9:50 a.m.
Salon E – Miami Marriot Biscayne Bay

Chairpersons: William Peatman, *Qualcomm*
Wooram Lee, *IBM T.J. Watson Research*

8:30 a.m.
J.1 **A 660 GHz Up-converter for THz Communications (Invited)**
W. R. Deal, K. Leong, A. Zamora, B. Gorospe, K. Nguyen, and X.B. Mei,
Northrop Grumman Corporation, Redondo Beach, USA

9:00 a.m.
J.2 **THz InP Bipolar Transistors – Circuit Integration and Applications (Invited)**
M. Urteaga[1], Z. Griffith[1], R. Pierson[1], P. Rowell[1], A. Young[1], H. Hacker[1], B. Brar[1], S.K. Kim[2], R. Maurer[2], and M.J.W. Rodwell[2],
[1]*Scientific Company, Thousand Oaks, USA*,
[2]*Dept of ECE, University of California Santa Barbara, Santa Barbara, USA*

9:30 a.m.
J.3 **Balanced Active Frequency Multipliers in D and G bands Using 250nm InP DHBT Technology**
S. Carpenter, Z. S. He, and H. Zirath,
Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Goteborg, Sweden

9:50 a.m.
End of Session J

10:00 a.m. – 10:30 a.m.
Coffee Break

SESSION K: Next Generation Wide Bandgap Technologies

8:30 a.m. – 9:40 a.m.
Salon ABCD –Miami Marriott Biscayne Bay

Chairpersons: Parrish Ralston, *Northrop Grumman*
Kazutaka Inoue, *Sumitomo*

8:30 a.m.
K.1 **Gallium Oxide Technologies and Applications (Invited)**
G. Jessen, K. Chabak, A. Green, N. Moser, J. McCandless, K. Leedy, A. Crespo, S. Tetlak, *Air Force Research Laboratory, Dayton, USA*

9:00 a.m.
K.2 **InAlN/GaN HEMT Using Microwave Annealing for Low Temperature Ohmic Contact Formation**
L. Chou[1], L. Peng[1], H.C. Wang[1], H. Chiu[1], H.T. Wang[1], D. Chiang[1], J. Chyi[2], [1]*Chang Gung University, Taoyuan City, Taiwan,* [2]*National Central University, Taoyuan City, Taiwan*

9:20 a.m.
K.3 **High Performance N-Polar GaN HEMTs with OIP3/P_{DC} ~12dB at 10GHz**
A. Arias[1], P. Rowell[1], J. Bergman[1], m. Urteaga[1], K. Shinohara[1], X. Zheng[2], H. Li[2], B. Romanczyk[2], M. Guidry[2], S. Weinecke[2], E. Ahmadi[2], S. Keller[2], U. Mishra[2], [1]*Teledyne Scientific Company, Thousand Oaks, USA,* [2]*University of California Santa Barbara, Santa Barbara, USA*

9:40 a.m.
End of Session K

10:00 a.m. – 10:30 a.m.
Coffee Break

SESSION L: RF Front End Control Circuits

10:30 a.m. – 12:00 p.m.
Salon E – Miami Marriott Biscayne Bay, USA

Chairpersons: Tomoya Kaneko, *NEC*
Don Kimball, *MaXentric Technologies*

10:30 a.m.
L.1 **SiGe BiCMOS Processes for Commercial RF Front-End-Module Applications (Invited)**
E. Preisler, K. Moen, J. Zheng, P. Hurwitz, S. Chaudhry, and M. Racanelli, *TowerJazz, Newport Beach, USA*

11:00 a.m.
L.2 **A 5-15 GHz Stacked I/Q Modulator with 15-19 dBm OP1dB and 26-30 dBm OIP3 in 45 nm SOI CMOS**
S. Zihir and G. Rebeiz, *University of California San Diego, La Jolla, USA*

11:20 a.m.
L.3 **Fully Differential High Input Power Handling Ultra-Wideband Low Noise Amplifier for MIMO Radar Application**
M. Sakalas[1], P. Sakalas[2, 3], N. Joram[1], and F. Ellinger[1], *[1]Chair for Circuit Design and Network Theory, Technische Universitat Dresden, Germany, [2]Chair for Electronic Devices and Integrated Circuits, Technische Universitat Dresden, Germany, [3]Fluctuation Research Laboratory, Center of Physical Sciences and Technologies, Vilnius, Lithuania*

11:40 a.m.
L.4 **A Novel Two-Dimensional Changeover GaN MMIC Switch for Electrically Selectable SPDT Multifunctional Device**
H. Mizutani[1], R. Ishikawa[2], and K. Honjo[2]
[1]Salesian Polytechnic, Tokyo, Japan, [2]The University of Electro-Communications, Tokyo, Japan

12:00 p.m.
End of Session L

12:00 p.m. – 1:30 p.m.
Break for Lunch

SESSION M: Photonic Integrated Circuits

10:30 a.m. – 11:50 a.m.
Salon ABCD – Miami Marriott Biscayne Bay

Chairpersons: Munehiko Nagatani, *NTT Corporation*
Craig Steinbeiser, *Qorvo*

10:30 a.m.
M.1 **Silicon-Photonics-Based Coherent Optical Subassembly (COSA) for Ultra-compact Coherent Transceiver (Invited)**
K. Kikuchi, K. Tsuzuki, S. Kamei, S. Yamanaka, S. Asakawa, T. Itoh, Y. Nasu, K. Takeda, K. Honda, Y. Kawamura, M. Jizodo, M. Takahashi, M. Usui, H. Mawatari, T. Saida, *NTT Corporation, Atsugi, Japan*

11:00 a.m.
M.2 **90mW, 4.4Vp-p, 11.35Gb/s MZM Driver Enabling Low-power Tunable Transmitter for SFP+ Module Application**
T. Nguyen, L. Li, G. Salamanca, O. Mizuhara, *Finisar Corporation, Sunnyvale, USA*

11:20 a.m.
M.3 **Ultra-high Bandwidth InP IQ Modulators for Next Generation Coherent Transmitter (Invited)**
Y. Ogiso, J. Ozaki, Y. Ueda, S. Kanazawa, H. Tanobe, S. Nakano, H. Yamazaki, T. Fujii, E. Yamada, N. Nunoya, N. Kikuchi, *NTT Corporation, Atsugi, Japan*

11:50 a.m.
End of Session M

SESSION N: High-Performance Circuits for Digital Communications

1:30 p.m. – 2:40 p.m.
Salon E – Miami Marriott Biscayna Bay

Chairpersons: Yuriy Greshishchev, *Ciena Corp.*
Waleed Khalil, *The Ohio State University*

1:30 p.m.
N.1 **High-Speed Data Converters and Their Applications in Optical Communication System (Invited)**
D. Cui, J. Cao, A. Nazemi, T. He, G. Li, B. Catli, K. Hu, H. Zhang, B. Rhew, S. Sheng, Y. Shim, B. Zhang, A. Momtaz, *Broadcom Limited, Irvine, USA*

2:00 p.m.
N.2 **A 56 Gb/s PAM-4 Linear Transimpedance Amplifier in 0.13 um SiGe BiCMOS Technology for Optical Receivers**
S. Bhagavatheeswaran[1], T. Cummings[2], E. Tangen[1], M. Heins[3], R. Chan[1], and C. Steinbeiser[1], *[1]IDP Group, Qorvo, Richardson, USA, [2]IDP Group, Qorvo, San Jose, USA,[3]The University of Texas at Dallas, Richardson, USA.*

2:20 p.m.
N.3 **Digital Post-Correction of Dynamic Nonlinearity in GaN HEMT Track-and-Hold Circuits**
S.W. Chung, P. Srivastava, X. Yang, T. Palacios, and H.-S. Lee *Microsystems Technology Laboratories, MIT, Cambridge, USA*

2:40 p.m.
End of Session N

Wednesday, October 25th, 2017

SESSION O: Late-Breaking News Papers I

1:30 p.m. – 3:10 p.m.
Salon ABCD – Miami Marriott Biscayne Bay, USA

Chairpersons: Zachary Griffith, *Teledyne Scientific*
Steve Huettner, *Nuvotronics*

1:30 p.m.
O.1 **Current Contours Based IMN Design Methodology for Broadband GaN Doherty Power Amplifiers**
K. Patel[1], H. Golestaneh[2], and S. Boumaiza[3], *[1]Wolfspeed, Research Triangle Park, USA, [2]Peraso Technologies, Toronto, Canada, [3]University of Waterloo, Waterloo, ON, Canada*

1:50 p.m.
O.2 **Coplanar Waveguide Performance Comparison on GaN-on-Si and GaN-on-SiC Substrates**
L. Cao[1], C.-F. Lo[2], H. Marchand[2], W. Johnson[2], and P. Fay[1]
[1]Department of Electrical Engineering, University of Notre Dame, Notre Dame, USA, [2]IQE, Taunton, USA

2:10 p.m.
O.3 **Surface-potential-based Gate-periphery-scalable Small-signal Model for GaN HEMTs**
S. Aamir Ahsan[1], S. Ghosh[1], S. Khandelwal[2], and Y. Singh Chauhan[1], *[1]Nanolab, Indian Institute of Technology Kanpur, India, [2]Department of Science and Engineering, Macquarie University, NSW, Australia*

2:30 p.m.
O.4 **Testbed for Phased Array Communications from 275 to 325 GHz**
T. Merkle[1], A. Tessmann[1], M. Kuri[1], S. Wagner[1], A. Leuther[1], S. Rey[3], M. Zink[1], H.-P. Stulz[1], M. Riessle[1], I. Kallfass[2], T. Kürner[3], *[1]Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany, [2]University of Stuttgart, Institute of Robust Power Semiconductor Systems, Stuttgart, Germany, [3]Technische Universität Braunschweig, Institute for Communications Technology, Braunschweig, Germany*

2:50 p.m.
O.5 **A Fully-Integrated S/C Band Transmitter in 45nm CMOS/ 0.2µm GaN Heterogeneous Technology**
M. LaRue[1], B. Dupaix[1], S. Rashid[1], T. Barton[2], S. Dooley[3], P. Watson[3], T. Quach[3], and W. Khalil[1]
[1]ElectroScience Laboratory, The Ohio State University, Columbus, USA, [2]University of Colorado Boulder, Boulder, USA, [3]Air Force Research Laboratory, Wright-Patterson Air Force Base, USA

3:10 p.m.
End of Session O

Wednesday, October 25th, 2017

SESSION P: Late-Breaking News Papers II

3:30 p.m. – 5:15 p.m.
Salon E – Miami Marriott Biscayne Bay, USA

Chairpersons: Jim Carroll, *NI-AWR Group*
Brian Moser, *Qorvo*

3:30 p.m.
Student Paper Competition Winner Pronouncement

3:35 p.m.
P.1 **A 28 GHz 480 elements Digital AAS using GaN HEMT Amplifiers with 68 dBm EIRP for 5G Long-range Base Station Applications**
T. Kuwabara[1], N. Tawa[1], Y. Tone[2], and T. Kaneko[1],
[1]NEC Corporation, Kawasaki, Kanagawa, Japan,
[2]NEC Platforms, Ltd., Chiyoda-ku, Tokyo, Japan

3:55 p.m.
P.2 **39GHz GaN Front End MMIC for 5G Applications**
B. Kim and V. Li, *Qorvo, Richardson, USA*

4:15 p.m.
P.3 **DC–60 GHz 4-Phase 25% Duty Cycle Quadrature Clock Generator**
N. Weiss[1], S. Shopov[1], P. Schvan[2], P. Chevalier[3], A. Cathelin[3], S. P. Voinigescu[1], *[1]ECE Department, University of Toronto, Toronto, Canada, [2]Ciena Corporation, Ottawa, Canada; [3]STMicroelectronics, Crolles, France*

4:35 p.m.
P.4 **A Compact, 37% Fractional Bandwidth Millimeter-wave Phase Shifter Using a Wideband Lange Coupler for 60-GHz and E-band Systems**
N. Hosseinzadeh and J. F. Buckwalter, *Department of Electrical and Computer Engineering, University Of California, Santa Barbara, Santa Barbara, USA*

4:55 p.m.
P.5 **Design and Linearity Analysis of a D-band Power Amplifier in 0.13 µm SiGe BiCMOS Technology**
Z. Hu, G. Sarris, C. De Martino, M. Spirito and E. McCune, *Electronic Research Laboratory, Delft University of Technology, Delft, The Netherlands*

5:15 p.m.
End of Session P

5:15 p.m.
Close of Symposium

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SYMPOSIUM CHECKLIST

☐ HOTEL RESERVATIONS

Click on the "Hotel" link on the conference website or go directly to:

https://aws.passkey.com/event/15933706/owner/2840/home

☐ SYMPOSIUM REGISTRATION

Click on the "Registration" link on the www.csics.org conference website or go directly to:

http://www.cvent.com/events/2017-ieee-compound-semiconductor-integrated-circuit-symposium-csics-/event-summary-19dcc70685bb4edca13b56fcb840e3f3.aspx

Advance registration deadline: September 23rd.

☐ EXHIBITOR INFORMATION

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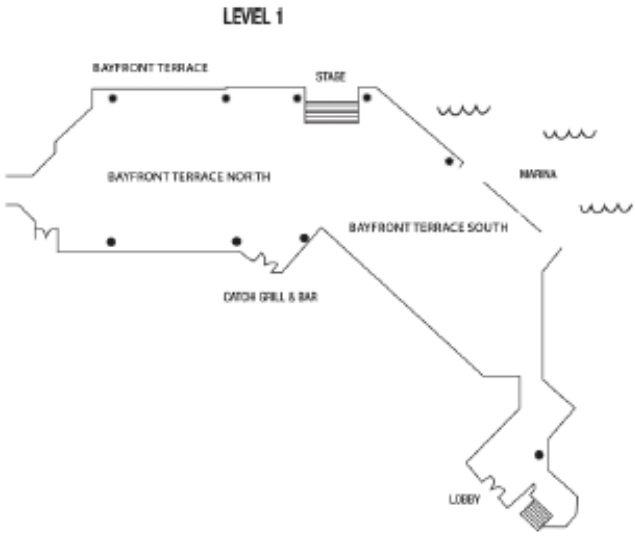
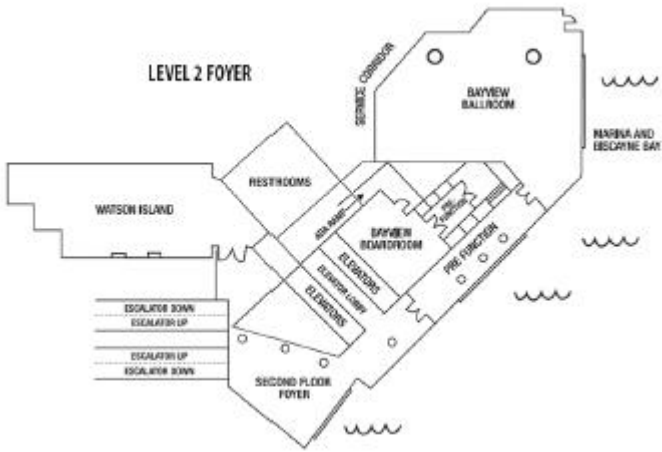
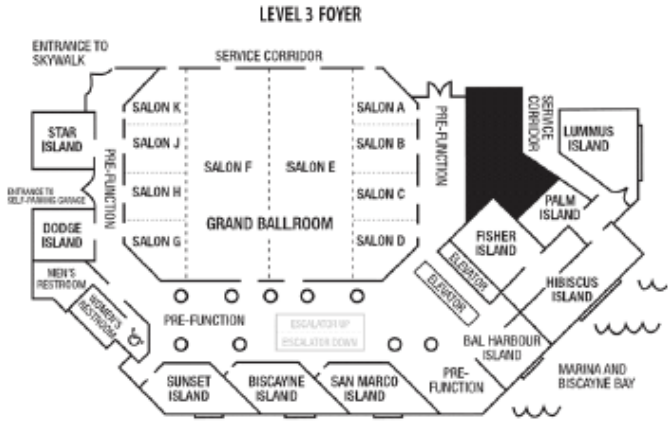
Miami Marriott Biscayne Bay Level 1



Miami Marriott Biscayne Bay Level 2



Miami Marriott Biscayne Bay Level 3



CSICS 2017 Technical Program

	Sunday October 22	Monday October 23	Tuesday October 24	Wednesday October 25	
7:00 - 7:30 AM	Reg. Short Course Breakfast Bayview Ballroom	Registration - 3rd Floor Foyer: Continental Breakfast Salon F	Registration - 3rd Floor Foyer: Technology Exhibition - Salon F: Exhibition Breakfast Salon F	Registration - 3rd Floor Foyer: Continental Breakfast Salon F	7:00 - 7:30 AM
7:30 - 8:00 AM					7:30 - 8:00 AM
8:00 - 8:30 AM	Short Course 1: Si Photonics Tech Watson; Primer 1: MMIC High Power Amplifier Design Hibiscus				8:00 - 8:30 AM
8:30 - 9:00 AM		Symposium Opening; Session A: Plenary Salon E	Session D High Speed Serial Links Salon E; Session E Adv Devices & Modeling Salon ABCD	Session J THz Systems & Applications Salon E; Session K Next Gen Wide Bandgap Tech Salon ABCD	8:30 - 9:00 AM
9:00 - 9:30 AM					9:00 - 9:30 AM
9:30 - 10:00 AM	AM Break				9:30 - 10:00 AM
10:00 - 10:30 AM		Break	Break	Break	10:00 - 10:30 AM
10:30 - 11:00 AM	Short Course 1: Si Photonics Tech Watson; Primer 2: Intro to Si Design Hibiscus	Session A: Plenary (cont'd) Salon E	Session F Adv mm-Wave & THz Si Circuits Salon E; Session G Thermal Char of GaN HEMTs Salon ABCD	Session L RF Front End Control Circuits Salon E; Session M Photonic Int Circuits Salon ABCD	10:30 - 11:00 AM
11:00 - 11:30 AM					11:00 - 11:30 AM
11:30 - 12:00 PM					11:30 - 12:00 PM
12:00 - 12:30 PM	Short Course Lunch Bayview Ballroom	Lunch (on your own)	Exhibition Luncheon Salon F	Lunch (on your own)	12:00 - 12:30 PM
12:30 - 1:00 PM					12:30 - 1:00 PM
1:00 - 1:30 PM					1:00 - 1:30 PM
1:30 - 2:00 PM	Short Course 1 Watson; Primer 2: Intro to Si Design Hibiscus	Session B GaN Systems & Components Salon E; Session C Char & Analysis of HBTs Salon ABCD	Session H III/V Solutions for 5G Applications Salon E; Session I GaN HEMT Modeling Salon ABCD	Session N High Perf Ckts for Dig Comm Salon E; Session O Late Breaking News I Salon ABCD	1:30 - 2:00 PM
2:00 - 2:30 PM					2:00 - 2:30 PM
2:30 - 3:00 PM					2:30 - 3:00 PM
3:00 - 3:30 PM	Registration - 3rd Floor Foyer: Break	Break	Break	Break	3:00 - 3:30 PM
3:30 - 4:00 PM	Short Course 1 Watson	Panel 1: Optics Invading Copper? The Future of Backplane Communication Salon E	Panel 2: Have North America & Europe handed the CMOS & comm. industries to Asia? Salon E	Session P Late Breaking News II Salon E	3:30 - 4:00 PM
4:00 - 4:30 PM	Break				4:00 - 4:30 PM
4:30 - 5:00 PM					4:30 - 5:00 PM
5:00 - 5:30 PM	Primer 2: Intro to Si Design Hibiscus	Exhibition Salon			5:00 - 5:30 PM
5:30 - 6:00 PM		Exhibition Opening Reception Salon F			5:30 - 6:00 PM
6:00 - 6:30 PM			Biscayne Lady Sunset Cruise 6-10pm		6:00 - 6:30 PM
6:30 - 7:00 PM					6:30 - 7:00 PM
7:00 - 7:30 PM	Opening Cocktail Bayview Ballroom				7:00 - 7:30 PM
7:30 - 8:00 PM					7:30 - 8:00 PM

Color Legend

Registration	Meals & Breaks	Tech Exhibit
Advanced Devices and Modeling		
Analog, RF, and Microwave ICs		
Millimeter-wave and THz Ics		
High-Speed Digital, Mixed Signal and Optoelectronic ICs		

Please note the times are approximate. Please refer to the detailed schedule on pp. 2 and 3.

CSICS Week – Schedule Overview

NOTES