36th IEEE COMPOUND SEMICONDUCTOR IC (CSIC) SYMPOSIUM

Program

Presenting:

CSICS: Where III-V meets Silicon

Oct 19th – Oct 22nd, 2014
Hyatt Regency La Jolla at Aventine

La Jolla, California, USA

CO- SPONSORED BY
The IEEE Electron Devices Society,
The IEEE Solid-State Circuits Society, and
The IEEE Microwave Theory and Techniques Society.

SYMPOSIUM

Sunday, October 19th, 2014
Short Course Continental Breakfast
SHORT COURSE 1: GaN HEMT Device Modeling
Short Course Lunch
REGISTRATION for Symposium
SHORT COURSE 2: Fundamentals of Power Conversion and Envelope Tracking
PRIMER COURSE 1: Fundamentals of A/D Converters
PRIMER COURSE 2: Introduction to Si RFIC Design
CSIC Symposium Opening Cocktail

Monday, October 20th, 2014
REGISTRATION
Continental Breakfast
SYMPOSIUM OPENING
SESSION A: Plenary Session
SESSION B: Advanced Low Noise and Mixer Technology
SESSION C: Thermal Management of GaN Devices
SESSION D: mm-Wave & THz Amplifiers
SESSION E: Advanced Optical Modulators
Exhibition Opening Reception
Technology Exhibition

Tuesday, October 21st, 2014
REGISTRATION
Technology Exhibition
Continental Breakfast
SESSION F: mm-Wave & THz Arrays
SESSION G: Emerging Technologies and Devices
PANEL SESSION 1: Will Silicon Photonics Rule the World of Optical Communications?
Exhibition Lunch
SESSION H: High-Speed Optical Communication Components
SESSION I: High Efficiency Power Amplifier Architectures
PANEL SESSION 2: Heterogeneous Integration – “Why is there III-V on my CMOS?”
DHS SPECIAL PRESENTATION: Overview of the Chemical Facility Anti Terrorism Standards Program
PANEL SESSION 3: My IC doesn’t work – whose fault is that?

Wednesday, October 22nd, 2014
REGISTRATION
Continental Breakfast
SESSION J: GaN Modeling
SESSION K: mm-Wave & THz Subsystems
SESSION L: Evaluation and Modeling of High-Power and High-Speed Devices
SESSION M: High Frequency Power Amplifiers
PANEL SESSION 4: Should universities continue to teach bipolar and III-V technologies?
SESSION N: Application of Next Generation Technologies
SESSION O: Mixed Signal Circuits
SESSION P: Breaking News Papers

Close of Symposium

AT A GLANCE

Sunday, October 19th, 2014

7:00 a.m. – 7:30 a.m.	**Mykonos A,B**
7:30 a.m. – 3:00 p.m.	Delphi A,B
12:00 p.m. – 1:00 p.m.	**Mykonos A,B**
2:00 p.m. – 8:00 p.m.	Grand Foyer
3:00 p.m. – 7:00 p.m.	Delphi A,B
1:00 p.m. – 2:30 p.m.	Athenia A,B
3:00 p.m. – 7:00 p.m.	Athenia A,B
7:00 p.m. – 8:30 p.m.	**Grand Foyer**

Monday, October 20th, 2014

7:00 a.m. – 5:00 p.m.	Grand Foyer
7:00 a.m. – 8:30 a.m.	**Foyer C**
8:30 a.m. – 10:00 a.m.	Aventine A,B,C
10:30 a.m. – 12:00 p.m.	Aventine A,B,C
1:30 p.m. – 2:50 p.m.	Aventine A,B,C
1:30 p.m. – 3:10 p.m.	Aventine D,E
3:30 p.m. – 4:50 p.m.	Aventine A,B,C
3:30 p.m. – 5:20 p.m.	Aventine D,E
6:00 p.m. – 7:30 p.m.	**Pavilion**
6:00 p.m. – 7:30 p.m.	**Pavilion**

Tuesday, October 21st, 2014

7:00 a.m. – 5:00 p.m.	Grand Foyer
7:00 a.m. – 4:00 p.m.	Pavilion
7:00 a.m. – 8:30 a.m.	**Pavilion**
8:30 a.m. – 9:40 a.m.	Aventine A,B,C
8:30 a.m. – 10:00 a.m.	Aventine D,E
10:30 a.m. – 12:00 p.m.	Aventine A,B,C
12:00 p.m. – 1:30 p.m.	**Pavilion**
1:30 p.m. – 2:50 p.m.	Aventine A,B,C
1:30 p.m. – 3:00 p.m.	Aventine D,E
3:30 p.m. – 5:00 p.m.	Aventine A,B,C
5:30 p.m. – 5:45 p.m.	Aventine A,B,C
5:45 p.m. – 7:15 p.m.	Aventine A,B,C

Wednesday, October 22nd, 2014

7:00 a.m. – 12:00 p.m.	Grand Foyer
7:00 a.m. – 8:30 a.m.	**Foyer C**
8:30 a.m. – 9:50 a.m.	Aventine A,B,C
8:30 a.m. – 10:10 a.m.	Aventine D,E
10:30 a.m. – 11:50 a.m.	Aventine A,B,C
10:30 a.m. – 11:50 a.m.	Aventine D,E
12:00 p.m. – 1:30 p.m.	Aventine A,B,C
1:30 p.m. – 3:00 p.m.	Aventine A,B,C
1:30 p.m. – 2:30 p.m.	Aventine D,E
3:30 p.m. – 5:05 p.m.	Aventine A,B,C

5:00 p.m. End of Symposium

Visit us at: http://www.csics.org

CHAIR'S MESSAGE

It is with great pleasure that I invite you to be a part of the 2014 IEEE Compound Semiconductor IC Symposium (CSICS). Thanks to the efforts of the many dedicated volunteers on the organizing committee and the generous support of the IEEE Electron Devices, Microwave Theory and Techniques, and Solid-State Circuits Societies, CSICS is proud to offer a world class technical program. For this 36th edition, CSICS will be held on October 19-22 in La Jolla, San Diego, California.

From its origins in 1978 as an international gathering for distinguished experts to present their latest results in GaAs IC technology and Monolithic Microwave Integrated Circuit design, the symposium has become much more and now embraces GaN, InP, SiGe, nanoscale CMOS, and many other emerging technologies. This convergence allows CSICS to offer a perfect blend of state of the art IC performance, innovative design techniques, and advanced device technologies. There are no other events in the world where you can see GaN HPAs, InP THz PAs, 100 Gb/s CMOS/SiGe transceivers, GaN HEMT power devices, and advances in compact modeling all presented alongside each other.

Following its tradition, CSICS will include presentations from worldwide submissions on all aspects of the technology, from materials and device fabrication and modeling to IC design and testing, high-volume manufacturing, and system applications. It will also feature the very latest results in RF/microwave, millimeter-wave, THz, analog mixed signal, and optoelectronic integrated circuits.

On Sunday prior to the symposium opening, CSICS will offer two topical short courses: "GaN HEMT Device Modeling" and "Fundamentals of Power Conversion and Envelope Tracking." Taught by leading experts, they are intended for both technologists and IC designers who seek a comprehensive understanding of the latest trends and techniques in GaN technology and circuit design. CSICS is also very proud to present two Primer courses this year instead of the customary single course: "Fundamentals of A/D Converters" and "Introduction to Si RFIC design." Both tutorials introduce the key concepts, techniques and practices for Si mixed signal and RF circuit design and are guaranteed to provide valuable insight for designers of all backgrounds.

As a complement to the technical program, the symposium includes numerous social events that allow participants to interact and network in a relaxed setting. These include the Sunday Evening Opening Reception, the Monday Evening Exhibition Opening Reception, and the Technology Exhibition Luncheon on Tuesday. CSICS also offers a daily breakfast and AM/PM coffee breaks on Monday through to Wednesday.

Please join us at the Compound Semiconductor IC Symposium in beautiful La Jolla, California.

Douglas S. McPherson, Chair

2014 IEEE CSICS

CORPORATE BENEFACTORS

This year, we are pleased to continue with the IEEE Compound Semiconductor IC Symposium Corporate Benefactors Program. This program allows companies interested in compound semiconductors to show their support for the Symposium by making contributions towards the cost of some of our social events.

These additional resources enable the Symposium to increase the quality of our event, as well as allowing companies an opportunity for some tasteful promotional activities. To discuss any of the benefactor opportunities in more depth, please contact:

Douglas S. McPherson
Tel: +1-613-670-3371
E-mail: dmcphers@ciena.com

As of this printing, the Corporate Benefactors for the 2014 Compound Semiconductor IC Symposium are as follows.

Gold Level Benefactor

RF Micro Devices

Silver Level Benefactors

Keysight Technologies

TriQuint Semiconductor

OMMIC

The Symposium Web Site www.csics.org has become a critical tool for the dissemination of information to prospective attendees, committee members and sponsors of the Symposium. Every year, the web site must be updated and maintained to effectively serve this purpose. We would like to acknowledge the following benefactor for providing the Symposium web site support for the 2014 CSIC Symposium:

Media Partners and Other Partner Conferences

IEEE ITHERM Conference
http://ieee-itherm.org/

International Symposium for Testing and Failure Analysis (ISTFA)
http://www2.asminternational.org/content/Events/istfa/index.jsp

IEEE Topical Symposium on
Power Amplifiers for Wireless Communications
http://pasymposium.ucsd.edu/

Comments regarding the web site or any publicity materials should be directed to the Publicity Chair, Brian Moser (bmoser@rfmd.com). Links to our corporate benefactors appear on our symposium website.

GENERAL INFORMATION

IEEE 36th CSIC Symposium
Oct 19th - Oct 22nd, 2014
Hyatt Regency La Jolla at Aventine
La Jolla, California, USA

REGISTRATION

	Advance (Received by Sept. 26th)	Regular (After Sept. 26th or on site)
Symposium Registration		
IEEE Member	$675	$725
Non-IEEE	$725	$825
IEEE Life-Member	$340	$340
Student	$340	$390
Special One Day - IEEE Member[1]	$340	$410
Special One Day - Non-IEEE[1]	$370	$430
Special One Day - Student[1]	$230	$260
Short/Primer Course		
Short Course 1+2	$500	$500
Short Course 1+2 Student	$250	$250
Primer Course 1+2	$250	$250
Primer Course 1+2 Student	$150	$150
Additional Items		
Guest Opening Cocktail Reception Ticket	$40	$40
Guest Exhibition Opening Reception Ticket	$80	$80
Adtl. Digest USB	$100	$100
Adtl. Short Course USB	$100	$100
Adtl. Primer Course Notes USB	$100	$100
Adtl. Full Access Exhibitor Registration	$295	$295
Adtl. Exhibits Only Registration	$195	$195

All fees are denominated in US$
Full Registration Includes: USB Digest, Opening Cocktail, all technical sessions, panels, exhibits, Exhibition Opening Reception, Exhibition Lunch, and all coffee breaks.
Short Course Registration Includes: Short Course Notes on USB, continental breakfast and Short Course Lunch
[1]Special One-day Registration Includes: USB only (no social functions)
Primer Course Registration includes: Primer Course Notes on USB Only

For **ADVANCE REGISTRATION,** click on the Symposium Registration link on the Symposium website (www.csics.org). Please note that advance registration ends on September 26th and fees go thereafter.

For registration and payment related questions, please contact:

IEEE/MCM: Shana Ramandi, CSICS Registrar,
445 Hoes Lane, Piscataway, NJ, 08854 USA
Tel: +1-732-465-5809
Toll Free (US or Canada) +1-800-810-4333
FAX : +1-732-465-6447
Email: csicsreg@ieee.org

The remittance is payable by checks in U.S. dollars only, by personal/company check drawn on a U.S. bank, U.S. currency or traveler's checks. Checks must be made payable to "IEEE/2014 CSICS" and must be encoded with the bank number, account number, and check number. Credit cards may also be used. Bank drafts from non-U.S. banks and foreign currency are unacceptable and will be returned.

When you register for the Conference, the contact information you provide (including your name, address, phone, and email address) may be shared with CSICS and, with your explicit consent, vendor exhibitors.

We urge you to pre-register to reduce your costs and to simplify your check-in at the Symposium. Your Technical Digest and registration materials will be ready for you at the Advance Registration Desk.

Registration Center:

The Symposium Registration Center is located in the Grand Foyer on Sunday through Wednesday. The operating hours will be as follows:

Short & Primer Course Registration only

Sunday, October 19th	7:00 a.m. – 8:30 a.m.
Sunday, October 19th	12:00 p.m. –1:00 p.m. (Primer)

Symposium Registration

Sunday, October 19th	2:00 p.m. – 8:00 p.m.
Monday, October 20th	7:00 a.m. – 5:00 p.m.
Tuesday, October 21st	7:00 a.m. – 5:00 p.m.
Wednesday, October 22nd	7:00 a.m. – 12:00 p.m.

Refund Policy:

All requests for refund/cancellation must be received in writing by September 19th, 2014. No refunds can be provided after this date. Cancellations will incur a US$50 administration fee. Please submit cancellation requests via email to csicsreg@ieee.org

Mail or Fax Completed Advance Registration Form to:

IEEE/MCM: Shana Ramandi, CSICS Registrar,
445 Hoes Lane, Piscataway, NJ, 08854 USA
Tel: +1-732-465-5809
Toll Free (US or Canada) +1-800-810-4333
FAX : +1-732-465-6447
Email: csicsreg@ieee.org

ACCOMMODATIONS

Hotel Reservations:

A block of rooms has been reserved at special discounted rates for Symposium participants at our headquarters hotel, Hyatt Regency La Jolla at Aventine. Enjoy a seaside destination with the charm of a European village and the panache of Southern California. Located in the city known as “The Jewel of the Pacific”, the hotel offers incomparable beaches, shopping, dining, galleries and attractions. Visit Stephen Birch Aquarium & Museum, spend a day kayaking, take a Baja Lobster or Wine tour, see live theater or shop San Diego’s trendy boutiques. Accommodations were recently refreshed and now include 42" flat screen TVs, an iHome stereo with iPod® docking station, in-room safe, complimentary daily newspaper, and Portico bath products. High-speed wireless Internet is available at nominal daily charge. Wheelchair accessible rooms are available.

Hotel Address and Phone Numbers:

Hyatt Regency La Jolla at Aventine
3777 La Jolla Village Drive,
San Diego, California, USA 92122
Tel: +1 858 552 1234
Fax: +1 858 552 6066
Web Site: http://www.hyattregencylajolla.com

While there are alternatives, we would like to remind attendees to please support the Symposium and fully enjoy all the activities on offer by staying at the official headquarters hotel. The Symposium relies on attendees staying at the conference Hotel to reduce the costs charged for the use of meeting rooms. Room reservations should be made as soon as possible, as there are a limited number available at the symposium rate. To qualify for the discounted rate reservations must be made by 5:00pm Pacific time, September, 12 2014. Rooms are available at the special Symposium group rate of US$179 per night. These rates do not include room taxes, which are %12.6.

To make a reservation, you can follow the link on the symposium website or contact the hotel direct at +1-858-552-1234 and ask for Reservations. Be certain to request the Special Group Rate for the IEEE CSIC Symposium or on-line at

https://resweb.passkey.com/Resweb.do?mode=welcome_gi_new&groupID=21374121

Rooms will be subject to availability and possibly be charged at higher rates. Check-in time is 3 p.m. or later; check-out time is 12 noon. If necessary, you may cancel your reservation 24 hours prior to arrival to avoid a one (1) night plus tax penalty charge.

TRANSPORTATION

Travel Arrangements:
Special Airfares:

Travel arrangements using the IEEE negotiated air carriers or the carriers of your choice can be made through World Travel, Inc. by calling between the hours of 8:00 a.m. and 5:30 p.m. EST Monday through Friday. Within the US and Canada, call (800) TRY-IEEE, (+1 800 879 4333); and outside of the US and Canada, call +1 717 556 1100. Or, you may visit their on-line travel service web site at http://www.ieee.org/travel. This secure site offers simple and convenient service through which you can search, reserve, and ticket your travel anytime, anywhere. Or you can e-mail your request to ieee@worldtravelinc.com.

IEEE corporate car rental discounts are also available to all attendees of the symposium. Discount codes below entitle attendees to receive special rates that have also been negotiated with Avis A606000, Budget X520000, Hertz 61368, and Enterprise NA24IE1.

Airport Transportation:

The San Diego International Airport/Lindberg Field (SAN) is about 10 miles from the Hyatt Regency La Jolla at Aventine. The airport accommodates domestic and international travel.

Airport Transfer:

Transfer to and from the airport can be made by means of shuttle or taxi. Express Shuttle or Cloud 9 Shuttle: Cost: approx. US$15.00 one way per person (subject to change) with pick up outside of baggage claim area.
Taxi: approx. US$35-US$45 one way with pick up outside of baggage claim area.

Driving Directions:

From San Diego Int'l Airport (10 miles)**:** Turn left on Harbor Drive, then left again on Laurel. Follow signs to I-5 North. Exit at La Jolla Village Drive and turn right. Turn right again at Lebon. Turn right on University Center Lane into the hotel.

http://hyattregencylajolla.publishpath.com/map-directions

ADDITIONAL INFORMATION

Distribution of Relevant Information:

The CSIC Symposium will provide an officially designated area near the registration desk to serve as the proper display area for those in need of space to disseminate free material relevant to the CSIC industry. Printed material of any form will not be allowed to be indiscriminately proliferated in the registration area, hallways, lobbies, or other gathering areas, in proximity to the Symposium, technical sessions, evening social activities, panel sessions, or the exhibition.

Photography:

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. No flash photography will be used. Video recording by participants and other attendees during any portion of the conference is not allowed without special prior written permission of IEEE. Photographs of copyrighted PowerPoint or other slides are for personal use only and are not to be reproduced or distributed. Do not photograph any such images that are labeled as confidential and/or proprietary.

Non Discrimination Policy

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws. For more information on the IEEE policy visit:

http://www.ieee.org/about/corporate/governance/p9-26.html?WT.mc_id=hpf_pol

Breakfast and Lunch Locations:

Breakfasts:

The location of breakfasts will be as follows:

Short Course Registrants (only) –
Sunday, October 19th Mykonos A,B

Symposium Registrants –
Monday, October 20th: Foyer C
Tuesday, October 21st: Pavilion
Wednesday, October 22nd: Foyer C

Lunches:

The location of lunches will be as follows:

Short Course Registrants (only) –
Sunday, October 19th: Mykonos A,B

Exhibition Luncheon –
Tuesday, October 20th: Pavilion

Coffee Breaks:

The location of coffee breaks will be as follows:

Short Course and Primer Course registrants (only) –
Sunday, October 19th — second floor conference level

Symposium Registrants –
Monday, October 20th: Grand Foyer
Tuesday, October 21st: Pavilion
Wednesday, October 22nd: Grand Foyer

Symposium Social Events:

SYMPOSIUM Opening Cocktail

We welcome you to San Diego on Sunday evening, October 19th from 7:00 p.m. to 8:30 p.m. in the Grand Foyer of the Hyatt Regency La Jolla at Aventine. Come and meet up with your old friends and make new acquaintances over cheese and wine, beer or soft drinks. One free admission is included with your registration including two drink tickets, and extra reception tickets may be purchased at registration for $40.

EXHIBITION OPENING RECEPTION

The exhibition opening reception will be held on Monday evening, October 20th from 5:30 p.m. to 7:30 p.m. in the Pavilion of the Hyatt Regency La Jolla at Aventine. Come along; visit with the exhibitors over light hors d'oeuvres and wine, beer, or soft drinks. One free admission is included with your registration, and extra reception tickets may be purchased at registration for $80.

EXHIBITION LUNCHEON

On Tuesday, October 21st at noon the Exhibition Luncheon will be hosted in the Pavilion. The lunch is free to all Symposium participants, so come along, visit with the exhibitors, ask questions, make deals and find out what is going on in our industry.

San Diego Attractions:

So much more than a pretty beach, San Diego is a laid-back spectacle of history, culture and wildlife. An estimated 1.36 million people call it their home, which stretches from the northern coasts of La Jolla and Pacific Beach, down to Mission Valley, Old Town and bustling Downtown San Diego. San Diego's roots trace back to the 1880s, and much of that historic character is retained in Downtown San Diego's Gas lamp District, not far from Manchester Grand Hyatt. The corridor is toasting to urban revival's finest hour, thanks to covert lounges and wine bars, trendy fashion boutiques and some of the finest craft beer selections on the planet (San Diegans love their IPAs). Equally legendary is the centrally located Balboa Park, home to 15 museums and the world-famous San Diego Zoo—one of three major animal attractions in the area. The 1,200-acre park is one of the oldest urban parks in the country, second only to New York's Central Park. Here, you find nearly all of the city's art galleries and theaters—including the famous Old Globe.

SYMPOSIUM HIGHLIGHTS

The technical program for the 2014 IEEE CSIC Symposium consists of 58 technical papers, four panel sessions, an industry exhibit, and two short courses “GaN HEMT Device Modeling” and “: Fundamentals of Power Conversion and Envelope Tracking.” We will also be offering two primer level classes, “Fundamentals of A/D Converters” and “Introduction to Si RFIC Design (Primer Courses 1 and 2).

This year we have invited 19 papers on a wide range of important topics encompassing advanced device engineering to circuit application using compound and other related semiconductor technologies.

Exciting new developments from a variety of compound semiconductor disciplines will be presented. This year there is considerable interest in GaN devices, heterogeneous integration, semiconductor processes for >100 GHz applications, and thermal management of high power devices. As always there is a tremendous amount of activity in wireless communications and military electronics.

Late-Breaking News Papers:

We have solicited papers containing late-breaking news for the Symposium Program. The times and locations of these presentations will be posted on the Symposium website.

Technical Digest:

Extra USB Technical Digests can be purchased by Symposium registrants through Advance Registration. A limited number of Digests USBs may also be available for sale at the Registration Desk. The cost of the USB ordered through Advance Registration or purchased on-site is $100.

Outstanding Paper Award:

The 2014 IEEE CSIC Symposium will select a contributed paper for the Outstanding Paper Award. All contributed regular papers (not the invited papers) will automatically be considered as candidates. Symposium attendees will have an opportunity to provide feedback through a Symposium questionnaire as well as to the Session Chairpersons. The award winner will be publicly announced shortly after this year's Symposium with the award formally presented during the next year's CSIC Symposium.

Student Paper Competition:

In recognition of the exceptional contributions made by students, CSICS is proud to hold its very first Student Paper Competition. To participate in the competition, an eligible student must submit a regular contributed paper naming, at a minimum, themselves and their principal supervisor as authors. The Student Paper Finalists must present their own papers at their assigned symposium session. We congratulate our six Student Paper Finalists for 2014 CSICS.

Short Course 1: “GaN HEMT Device Modeling”

Short Course Description

Most of the models used by IC designers in the III-V world are equivalent circuit based models (ECM) because of their easy implementation in circuit simulators. The first III-V devices used for microwave ICs (MMICs) were GaAs FETs and HEMTs, with GaAs MHEMTs and InP HEMTS being used at millimeter wave frequencies (> 40GHz). In addition to these models, physics based and behavioral models were also developed for these devices. During the last ten years, GaN technology has been positioning itself to displace GaAs as the main technology used for MMIC designs. This course focuses on the three major modeling methods and specific issues related to GaN HEMT technologies.

During the 1980s and 1990s when the initial analog GaAs FET device technologies were being developed, various models were derived to characterize these new devices. Some of these models included the Curtice Cubic, Statz-Raytheon, Angelov, and the EEHEMT model developed by Agilent (then Hewlett-Packard), and the Root Model. Designers coming of age in this era needed to develop a familiarity with these models and learn under what circumstances they were valid. As GaN FET technology emerged in the 2000s, many of these same models and new physics based models were used to model the new devices. The questions that designers may now ask are how well these models work for GaN devices, what specific issues are device modelers encountering, and what modifications need to be done to generate valid models.

The course opens with a discussion of equivalent circuit based models and how they apply to GaN HEMTs. Specific topics addressed in this first section include the characteristics of the various nonlinear elements that are used in these models and how to they fit into a nonlinear model. Particular emphasis will be placed on the Angelov model. The second section covers GaN Physics based models and addresses how these models have evolved from principles of solid state physics. These models provide great insight into how equations governing solid state physics can be applied to specific nonlinear models. The third part of the course covers compact and behavioral models, focuses on the equations governing these models, and the extraction and fitting techniques used to realize them. All sections of the course will compare GaAs and GaN technologies in order to show how device and modeling technology has evolved over the years.

Short Course 2: “Fundamentals of Power Conversion and Envelope Tracking”

Short Course Description

Microwave power amplifier designers have typically designed for continuous wave and pulsed power systems with limited duty cycles. As more complex modulation schemes such as multi-level QAM become more prevalent in wireless communication systems, RF power amplifier designers will have to learn techniques to optimize system efficiency. QAM systems are characterized by inputs with peak-to-average power ratios (PAPR) on the order of 6-7dB so efforts are being made to alleviate the loss in efficiency caused by the power amplifiers not operating at their optimum load. A proposed solution to this problem is to use envelope tracking (ET) whereby the drain bias supply of the power amplifier is increased or decreased to maximize efficiency as input power varies. Issues that prevent the implementation of envelope tracking in current systems include the loss of efficiency due to the added circuitry to implement the scheme and bandwidth limited by device switching speed.

Recent device research in GaN and SiC technology has focused on high power switching devices for power supply applications because of their potential to maintain high efficiency at fast switching speeds. In addition to common power supply applications such as buck converters, and inverters, GaN device technology has been proposed for use in DC-to-DC converters. DC/DC converters are the key components for altering the power amplifier drain voltages in tracking schemes. In order to develop envelope tracking systems, designers should have a good working knowledge of how DC/DC converters work and how to improve their efficiency.

The first part of this course reviews the principles of power conversion and specifically addresses the nuances of DC/DC conversion. Topics covered include the basics of boost and buck converters, the design of DC/DC converters and the characteristics and figures of merit of power devices. These fundamentals will be used to lead into the second part of the course which discusses the specifics of envelope tracking circuits with state-of-the-art design examples.

Direct questions to:
Harris P. Moyer, Short Courses Coordinator
HRL Laboratories, LLC.
(310) 317-5784
hpmoyer@hrl.com

Panel Sessions:

This year we have four exciting Panel Sessions on Tuesday October 21st and Wednesday October 22nd. These are intended to be timely, thought-provoking, educational, and hopefully controversial. The four panel topics are as follows:

PANEL SESSION 1:
Will Silicon Photonics Rule the Optical Communications World?
Tuesday, October 21st, 10:30 a.m. - 12:00 p.m.

PANEL SESSION 2:
Heterogeneous Integration – “Why is there III-V on my CMOS?”
Tuesday, October 21st, 3:30 p.m. - 5:00 p.m.

PANEL SESSION 3:
My IC doesn’t work – Whose fault is that?
Tuesday, October 21st, 5:30 p.m. - 7:00 p.m. (cash bar)

PANEL SESSION 4:
Should Universities Continue to Teach Bipolar and III-V Technologies?
Wednesday, October 22nd, 12:00 p.m. - 1:30 p.m.

Please see the "Symposium Program" section later in this brochure for more complete descriptions of each of these Panel Sessions (listed according to day and time).

Technology Exhibition:

The 2014 IEEE CSICS Technology Exhibition will be held on Monday evening October 20th and Tuesday the 21st in the Pavilion and is open to all Symposium registrants. The combined exhibition gives companies and attendees access to the entire array of compound semiconductor products and services, i.e., materials, manufacturing, device technology, integrated circuits, as well as the latest information

on modeling and design simulation tools. As of printing, this year's exhibitors are:

Accel-RF Corp.
Integrand Software, Inc.
Nuhertz Technologies, LLC
Sonnet Software, Inc.
Rhode & Schwarz GmbH
Kyocera, Inc.
Agilent Technologies
Maury Microwave Corp.
Presidio Components Corp.
StratEdge Corp.
NI-AWR Group

The Exhibition will feature informative and interesting displays with corporate representatives on hand between the hours of 6:00 p.m. and 8:00 p.m. on Monday, October 20th, and between 7:00 a.m. and 4:00 p.m. on Tuesday, October 21st. The Exhibition will also host the Exhibition Opening Reception from 6:00 p.m. until 7:30 p.m. on Monday evening and the Exhibition Luncheon from 12:00 noon to 1:30 p.m. on Tuesday. The Exhibition Opening Reception, the Exhibition Luncheon, and the Tuesday coffee breaks will be held in the exhibition area in the Pavilion.

To participate in the Exhibition, please contact Candi Wooldridge (MP Associates), candi@mpassociates.com, (303) 530-4562. Please visit the Symposium website at www.csics.org for additional information.

Short Courses

Sunday, October 19th, 2014
Hyatt Regency La Jolla at Aventine
Delphi A,B
7:30a.m. - 7:00p.m.

Course Coordinator:

Harris Moyer
HRL Laboratories, LLC.
310-317-5784
hpmoyer@hrl.com

"GaN HEMT Device Modeling"

The course opens with a discussion of procedures to extract Large-Signal Equivalent Circuit Models (LS ECM) for microwave FET transistors. A short description will be given how the EC models can be constructed and implemented in the CAD tools. Modeling flow will be shown, starting with the direct extraction of important device and model parameters. Examples of large-signal models of GaN, GaAs transistors will be discussed. Special attention will be paid on the modeling of GaN HEMT devices.

The second section of the course will survey the pros and cons of all three modeling approaches and demonstrate that physics-based device models have advanced to the point that they can now be successfully integrated into circuit and system simulators. Thus, they can provide an alternative to the commonly used equivalent circuit-based models. The physics-based device models are developed a-priori from the semiconductor device equations and are formulated in a simplified and efficient manner so that solution time is minimized. A new physics-based model for nitride-based HFETs has been developed and will be discussed.

Finally, an in-depth overview of two complementary and recent "compact" and "behavioral" approaches to nonlinear simulation models of GaN transistors is presented. The first approach is a new time-domain III-V transistor model, *DynaFET*, featuring dynamic self-heating and trapping effects, and its systematic identification from large-signal waveform measurements using advanced artificial neural network (ANN) technology. The second is based on applications of arbitrary load-dependent X-parameters for a native frequency domain model. Both methods are enabled by the power and versatility of the nonlinear vector network analyzer (NVNA) instrument working in concert with load-pull or active source injection at each port of the transistor. These approaches will also be contrasted with more conventional approaches, including those based on pulsed measurements. The course is presented by Dr. Iltcho Angelov, Dr. Robert Trew, and Dr. David Root, all renowned experts in the modeling world.

Topics Covered and Instructors:

1) Equivalent Circuit Based Modeling Techniques for GaN HEMTs – Iltcho Angelov, Chalmers University
2) GaN Physics Based Modeling Techniques – Robert Trew, North Carolina State University
3) Compact and Behavioral Modeling Techniques for GaN Devices – David Root, Agilent Technologies

"Fundamentals of Power Conversion and Envelope Tracking"

This short course starts with an introduction to circuits and the operation of switched-mode power converters, followed by steady-state and dynamic analysis and modeling techniques. Loss mechanisms are then examined, including conduction and switching losses, and dependences on device characteristics. In envelope tracking applications, switched-mode power converters are used as supply modulators for radio-frequency power amplifiers (RFPA) requiring simultaneously high efficiency and very high tracking bandwidth capabilities. The first part of the course also presents advances in the integration of high-performance switched-mode and linear-assisted power converters in a GaN process. Circuit design techniques are presented for integrated GaN power converters together with simulation and experimental prototype examples which operate with peak efficiencies greater than 90% when operating at 10-200 MHz switching frequencies.

The second section of this course will focus primarily on the envelope tracking method for both base-stations and mobile terminals (e.g. smart phones). Circuits for supply modulators and how they can be applied to various classes of microwave power amplifiers (e.g. Class AB, F, etc.) will be covered. Wideband stability of the envelope amplifier will be discussed and will include RC shunt snubber circuits, low output impedance, dual-feedback, hysteresis, dead-band, and the R.D. Middlebrook loop-gain & phase margin analysis & measurement. Linearization methods tailored to this technique will be presented. The challenge of modulation bandwidth limitation will be addressed with several solutions. Finally, the issue of receive band noise, especially in multi-carrier systems, will be presented with possible solutions. The power conversion fundamentals section will be taught by Dr. Dragan Maksimovic and the envelope tracking portion will be covered by Mr. Donald Kimball. Both are known experts in their field.

Topics Covered and Instructors:

1) Power Conversion Fundamentals and Technology – Dragan Maksimovic, University of Colorado, Boulder
2) Envelope Tracking in Modern Communication Systems – Donald Kimball, MaXentric Technologies, LLC.

Short Course Schedule

The short courses will be held on Sunday October 19th in Delphi A,B. A continental breakfast is available to all registered Short Course attendees and instructors. The first course "GaN HEMT Device Modeling" will begin at 7:30 am and finish at 2:45 pm. A lunch will be provided as well as morning and afternoon refreshment breaks.

The second short course "Fundamentals of Power Conversion and Envelope Tracking" will begin at 3:00 pm and finish at 7:00 pm and includes a refreshment break. All participants are invited to join the Symposium Opening Reception at 7:00 pm in the Grand Foyer.

Short Course I – GaN HEMT Device Modeling

Delphi A,B

7:00 a.m.	**Registration and Breakfast**
7:30 a.m.	**Introduction and Overview**
7:45 a.m.	**Equivalent Circuit Based Modeling Techniques for GaN HEMTs** Iltcho Angelov, Chalmers University
9:30 a.m.	**Coffee Break**
10:00 a.m.	**GaN Physics Based Device Modeling Techniques** Robert Trew, North Carolina State University
11:45 a.m.	**Lunch**
12:45 p.m.	**Compact & Behavioral Modeling Techniques for GaN Devices** David Root, Agilent Technologies
2:30 p.m.	**Coffee Break and Q&A**
2:45 p.m.	**Close of Short Course**

Short Course II – Fundamentals of Power Conversion and Envelope Tracking

Delphi A,B

3:00 p.m.	**Introduction and Overview**
3:15 p.m.	**Power Conversion Fundamentals and Technology** Dragan Maksimovic, University of Colorado, Boulder
4:45 p.m.	**Coffee Break**
5:15 p.m.	**Envelope Tracking in Modern Communication Systems** Donald Kimball, MaXentric Technologies, LLC.
6:45 p.m.	**Questions and Discussion**
7:00 p.m.	**Close of Short Course**

Who Should Attend

This first course is intended to appeal to both technologists and circuit designers of all backgrounds who have an interest in understanding the various types of GaN models available and their application space. Each lecture will highlight the relevant state-of-the-art models and provide insight into developments that lie ahead as the models are further refined. While the emphasis is on the specific GaN models in current use, comparisons with GaAs models will be provided and general device model extraction techniques will be discussed.

The second course will be of interest to scientists and engineers who would like to better understand DC power conversion, how it may be applied to envelope tracked power amplifiers, and the use of envelope tracking in modern communications. The first lecture will introduce the fundamentals necessary to understand envelope tracking systems while the second lecture will provide an introduction to envelope tracked power amplifiers with practical examples.

Short Course Pre-Registration

So that we may properly plan for attendance, we encourage you to pre-register for the Short Courses. A limited number of Short Course registrations will be available on site Sunday October 19th 7:00 am – 8:00 am. The registration fee for Short Course I and II is $500 for professionals and $250 for students. This includes attending the lectures, notes for both Short Courses available for download and on a USB stick, a continental breakfast, a lunch and morning/afternoon refreshments during breaks. Additional copies of the Short Course Notes on USB may be purchased for $100 each.

Primer Courses

Sunday, 19 October 2014 in Athenia A,B
1:00 p.m. – 7:00 p.m.

Primer Course I--Fundamentals of A/D Converters

Instructor: Dr. Hui Pan
Broadcom
Irvine, CA

Course Objective and Description:

As RF/IF sampling, software defined radio (SDR), Full-Band Capture (FDC), and Electronic Dispersion Compensation (EDC) have become reality in nanoscale CMOS technology, RF circuits and optical components are increasingly being replaced by digital signal processors (DSPs). As a result, understanding the principles and design of data converters has taken on much greater significance for RF and optical engineers. As there are very distinct differences between continuous-time RFIC/MMIC circuits and discrete-time data converters, the learning curve is steep for new designers. Even for experienced data converter designers, it can be a major challenge to make the best choice of architecture and circuits, when there are so many options. This primer on A/D converter (ADC) design aims to lower the barrier to

entry for newcomers, while providing new angles for incumbent practitioners by presenting the key aspects of ADCs from quantization fundamentals to interleaving techniques and circuit implementations. Using a logical and unified framework, the course will provide a comprehensive overview of the similarities, strengths, and limitations of the various ADC building blocks and their underlying principles. The course opens with a survey of the latest developments, followed by a derivation of the various ADC types and constituent blocks from a signal folding perspective. Track-and-Holds (T/Hs) are then introduced as a means to improve the dynamic performance of quantizers, with pipeline and interleaving techniques applied to increase the throughput. The performance metrics are defined, with the impact of the major architecture and circuit imperfections reviewed and their impact on spectral performance assessed. Some techniques to mitigate the imperfections are also shown with design examples of flash, pipeline, and SAR ADCs to be covered at the end of the talk.

The course instructor, Doctor Hui Pan, received the B.E. degree from Tsinghua University, Beijing, China, in 1983 and the Ph.D. degree from UCLA in 1999, both in Electrical Engineering. He joined Broadcom in 1999, where he is currently a Technical Director and Distinguished Engineer working on high speed wireline communication circuits and systems. Dr. Pan was the recipient of the 1998 Analog Devices Outstanding Student Designer Award and an Honorable Mention at the 2000 Design Automation Conference. He served on ISSCC TPC 2006 – 2010.

Primer I Agenda:

1:00 P.M. **Introduction and Overview**

1:05 P.M. **Quantization algorithms and architectures**

1:30 P.M. **A/D converter building blocks and integration**

1:45 P.M. **Performance metrics and measurements**

2:00 P.M. **Circuit imperfections and the performance impacts**

2:10 P.M. **Flash, Pipeline and SAR ADCs**

2:30 P.M. **Close of Primer I**

Primer Course II-- Introduction to Si RFIC Design

Instructor:

Prof. Waleed Khalil
The Ohio State University
Columbus, OH

Course Objective and Description:

Silicon Radio Frequency Integrated Circuits (RFICs) are the dominant technology for wireless transceivers and sensors due to their low cost, ease of integration with digital functions, and excellent RF performance. This course is intended for semiconductor professionals of all technical backgrounds who wish to learn or refresh their understanding of the fundamentals of designing the principal circuit building blocks in radio and radar SoCs. The primer will begin with an overview of the nanoscale CMOS and SiGe NPN transistors and integrated passives from an RF perspective, analyzing key concepts in modeling and noise behavior. This will be followed by an overview of

the RFIC design approach and a comparison to traditional III-V MMIC design. In so doing, the intent is to provide guidance on how the circuit design process differs and to enlighten attendees on subjects such as transistor sizing, proper layout practices, parasitic reduction strategies and transceiver integration. In the second part of the primer, the focus will shift to the key building blocks that make up Silicon based integrated transceivers. Among the blocks to be covered are PAs, LNAs, Mixers, Modulators, VCOs, and VGAs. For each one, designers are confronted with a variety of different circuit topologies, each with its attendant strengths and performance metrics. Making the right choice very much depends on having an awareness of what the options are, good specmanship and how the block will affect overall transceiver performance. Finally, the course will cover simulation methodologies and provide examples of circuit blocks implemented in both CMOS and SiGe technology.

The course instructor, Doctor Waleed Khalil, is currently serving as an assistant professor at the ECE department and the ElectroScience Lab, The Ohio State University. Prior to joining Ohio State, Prof. Khalil spent 16 years at Intel Corporation where he held various technical and leadership positions in wireless and wireline communication groups. While at Intel, he established Intel's first analog device modeling methodology for mixed signal circuit design and also contributed to the development of Intel's first RF process technology. Prof. Khalil's current research areas of interest include: RF and mm-wave circuits and systems, sub-THz circuits, front-end actives and passives, high performance clocking circuits, GHz A/D and D/A circuits.

Primer II Agenda:

3:00 P.M. **Introduction and Overview**

3:35 P.M. **Si RFIC technology and devices**

4:00 P.M. **Design Approach in RF CMOS versus III-V MMICs**

4:30 P.M. **Coffee Break**

5:00 P.M. **Transmitter building blocks**

5:40 P.M. **Receiver building blocks**

6:20 P.M. **Clock Generation**

7:00 P.M. **Close of Primer II**

Primer Course Coordinator:
Douglas S. McPherson, Primer Course Organizer and Chair
Ciena Corporation
3500 Carling Ave
Ottawa, ON K2H 8E9 Canada
(613) 670-3371 dmcphers@ciena.com

Student Paper Finalists

Competition Chair: Prof. Waleed Khalil
The Ohio State University
Columbus, OH

Presentation Schedule for the six Student Paper Finalists:

Monday, October 20, 2:30 p.m. (Aventine A,B,C)

B.4 **A up to 100 GHz Broadband Mixer with Cascaded Distributed Amplifier**
Y. Li[1,2], Y. Xiong[2], W. Goh[1], [1]*Nanyang Technological University, Singapore,* [2]*Terahertz Research Center, CAEP, Chengdu, China.*

Monday, October 20, 2:30 p.m. (Aventine D,E)

C.4 **Thermal Interface Resistance Measurements for GaN-on-Diamond Composite Substrates**
J. Cho[1], Y. Won[1], D. Francis[2], M. Asheghi[1], K. Goodson[1], [1]*Stanford University, Stanford, United States,* [2]*Element Six Technologies, Santa Clara, United States*

Tuesday, October 21, 9:30 a.m. (Aventine D,E)

K.3 **An Active Double-Balanced Down-Conversion Mixer in InP/Si BiCMOS Operating from 70-100 GHz**
J. J. McCue[1], M. Casto[1,2], J. C. Li[3], P. Watson[2], W. Khalil[1], [1]*The Ohio State University, Columbus, United States,* [2]*The Air Force Research Laboratory, Wright-Patterson AFB, United States,* [3]*HRL Laboratories, LLC, Malibu, United States*

Wednesday, October 22, 10:30 a.m. (Aventine A,B,C)

L.1 **An evaluation of extraction methods for the emitter resistance for InP DHBTs**
T. Nardmann[1], J. Krause[1], M. Schroter[2], [1]*TU Dresden, Dresden, Germany,* [2]*UC San Diego, La Jolla, United States*

Wednesday, October 22, 11:30 a.m. (Aventine D,E)

M.4 **Investigation of various envelope complexity linearity under modulated stimulus using a new envelope formulation approach**
F. Ogboi[1], P. Tasker[1], M. Akmal[1], J. Lees[1], J. Benedikt[1], S. Bensmida[2], K. Morris[2], M. Beach[2], J. McGeehan[2], [1]*Cardiff University , Cardiff, United Kingdom,* [2]*University of Bristol, Bristol, United Kingdom*

Wednesday, October 22, 1.30 p.m. (Aventine D,E)

O.1 **1700 pixels per inch (PPI) Passive-Matrix Micro-LED Display Powered by ASIC**
W. Chong[1], W. Cho[1], Z. Liu[1], C. Wang[2], K. Lau[1], [1]*Hong Kong University of Science and Technology, Hong Kong,* [2]*3C Limited, Hong Kong*

CSIC Symposium Opening
Cocktail Hour

Grand Foyer
7:00 p.m. - 8:30 p.m.

SYMPOSIUM PROGRAM

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – Grand Foyer– Hyatt Regency La Jolla at Aventine
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Foyer C

SYMPOSIUM OPENING

8:30 a.m. – 9:00 a.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Opening Remarks
2014 Symposium General Chair
Douglas S. McPherson, *Ciena Corporation*

Technical Program Overview
2014 Technical Program Chair
Charles Campbell, *TriQuint Semiconductor*

SESSION A: PLENARY SESSION

9:00 a.m. – 11:45 a.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: Harris Moyer, *HRL Laboratories*
Jim Carroll, *NI-AWR Group*

9:00 a.m.
A.1 **Evolution of Multi-Gigabit Wireline Transceivers in CMOS (Invited)**
I. Fujimori, *Broadcom Corporation, Irvine, United States,*

9:30 a.m.
A.2 **FD-SOI Technology Development and Key Device Characteristics for Fast, Power Efficient, Low Voltage SoCs (Invited)**
J. Hartmann, *ST Microelectronics, Crolles, France*

10:00 a.m. - 10:15 a.m.
Coffee Break

10:15 a.m.
A.3 **Materials and Integration Strategies for Modern RF Integrated Circuits (Invited)**
D. Green, *DARPA, Arlington, United States*

10:45 a.m.
A.4 **Future of GaN RF Technology in Europe (Invited)**
H. Blanck, *United Monolithic Semiconductors, Ulm, Germany*

11:15 a.m.
A.5 **GaN for Next Generation Electronics (Invited)**
P. Saunier, *TriQuint Semiconductor, Richardson, United States*

Monday, October 20th, 2014

11:45 a.m.
End of Session A

12:00 p.m. – 1:30 p.m.
Break for Lunch

SESSION B: Advanced Low Noise and Mixer Technology

1:30 p.m. – 2:50 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: Gilberto A. De la Rosa, *Anadigics*
Tomoya Kaneko, *NEC*

1:30 p.m.
B.1 **An InP MMIC Process Optimized for Low Noise at Cryo**
P. Nilsson[1], J. Schleeh[2], N. Wadefalk[2], P. Starski[1], G. Alestig[1], J. Halonen[1], B. Nilsson[1], H. Zirath[1], J. Grahn[1], *[1]Chalmers University, Göteborg, Sweden, [2]Low Noise Factory AB, Mölndal, Sweden*

1:50 p.m.
B.2 **Single Chip RF Variable Gain Low Noise Amplifier**
B. Hou, Y. Zhao, E. Newman, S. Zhang, *Analog Devices, Wilmington, United States*

2:10 p.m.
B.3 **A 0.05-26 GHz Direct Conversion I/Q Modulator MMIC**
E. Iverson, M. Feng, *University of Illinois at Urbana-Champaign, Urbana, United States*

2:30 p.m.
B.4 **A up to 100 GHz Broadband Mixer with Cascaded Distributed Amplifier**
Y. Li[1,2], Y. Xiong[2], W. Goh[1], *[1]Nanyang Technological University, Singapore, [2]Terahertz Research Center, CAEP, Chengdu, China.*

2:50 p.m.
End of Session B

SESSION C: Thermal Management of GaN Devices

1:30 p.m. – 3:10 p.m.
Aventine D,E – Hyatt Regency La Jolla at Aventine

Chairpersons: Hooman Kazemi, *Nuvotronics*
Avinash Kane, *Booz Allen Hamilton*

1:30 p.m.
C.1 **Optimizing GaN-on-Diamond Transistor Geometry for Maximum Output Power**
J. Pomeroy, M. Kuball, *University of Bristol, Bristol, United Kingdom*

1:50 p.m.
C.2 **Progress on Phase Separation Microfluidics**
D. Agonafer, J. Palko, Y. Won, K. Lopez, T. Dusseault, J. Gires, M. Asheghi, J. Santiago, K. Goodson, *Stanford University, Stanford, United States*

Monday, October 20th, 2014

2:10 p.m.
C.3 **High Resolution Thermal Characterization of Power GaN HEMTs Using Ultra-fast Transient Thermoreflectance Imaging and Micro-Raman Thermography**
K. Maize[1], S. Choi[2], L. Yates[2], D. Kendig[3], S. Graham[2], A. Shakouri[1], *[1]Purdue University, West Lafayette, United States, [2]Georgia Institute of Technology, Atlanta, United States, [3]Microsanj Inc., San Jose, United States*

2:30 p.m.
C.4 **Thermal Interface Resistance Measurements for GaN-on-Diamond Composite Substrates**
J. Cho[1], Y. Won[1], D. Francis[2], M. Asheghi[1], K. Goodson[1], *[1]Stanford University, Stanford, United States, [2]Element Six Technologies, Santa Clara, United States*

2:50 p.m.
C.5 **Microfluidics Heat Exchangers for High Power Density GaN on SiC**
Y. Won, F. Houshmand, D. Agonafer, M. Asheghi, K. Goodson, *Stanford University, Stanford, United States*

3:10 p.m.
End of Session C

3:00 p.m. - 3:30 p.m.
Coffee Break

SESSION D: mm-Wave & THz Amplifiers

3:30 p.m. – 4:50 p.m.
Aventine A,B,C– Hyatt Regency La Jolla at Aventine

Chairpersons: Arun Natarajan, *Oregon State University*
Hooman Kazemi, *Nuvotronics LLC*

3:30 p.m.
D.1 **A 23.2dBm at 210GHz to 21.0dBm at 235GHz 16-way PA-cell combined InP HBT SSPA MMIC**
Z. Griffith, M. Urteaga, P. Rowell, R. Pierson, *Teledyne Scientific Company, Thousand Oaks, United States*

3:50 p.m.
D.2 **Backside Process Free Broadband Amplifier MMICs at D-Band and H-Band in 20 nm mHEMT Technology**
T. Merkle[1], A. Leuther[1], S. Koch[3], I. Kallfass[1,2], A. Tessmann[1], S. Wagner[1], H. Massler[1], M. Schlechtweg[1], O. Ambacher[1], *[1]Fraunhofer Institute for Applied Solid State Physics (IAF), Freiburg, Germany, [2]University of Stuttgart, Stuttgart, Germany, [3]Independent Scholar, Oppenweiler, Germany*

4:10 p.m.
D.3 **A Broadband 220-320 GHz Medium Power Amplifier Module**
A. Tessmann, A. Leuther, V. Hurm, H. Massler, S. Wagner, M. Kuri, M. Zink, M. Riessle, H. Stulz, M. Schlechtweg, O. Ambacher, *Fraunhofer IAF, Freiburg, Germany*

4:30 p.m.
D.4 **A 200mW SSPA from 76-94GHz, with peak 28.9% PAE at 86GHz**
Z. Griffith, M. Urteaga, P. Rowell, R. Pierson, *Teledyne Scientific Company, Thousand Oaks, United States*

4:50 p.m.
End of Session D

SESSION E: Advanced Optical Modulators

3:30 p.m. – 5:20 p.m.
Aventine D,E – Hyatt Regency La Jolla at Aventine

Chairpersons: Craig Steinbeiser, *TriQuint Semiconductor*
Munehiko Nagatani, *NTT Photonics Laboratories*

3:30 p.m.
E.1 **Linear Optical Modulator for DAC-based Coherent Fiber Communications Systems (Invited)**
H. Yamazaki, *NTT Photonics Laboratories, Atsugi, Kanagawa, Japan*

4:00 p.m.
E.2 **A Compact Low-Power 224-Gb/s DP-16QAM Modulator Module with InP-based Modulator and Linear Driver ICs (Invited)**
N. Itabashi, T. Tatsumi, T. Ikagawa, N. Kono, M. Seki, K. Tanaka, K. Yamaji, Y. Fujimura, K. Uesaka, T. Nakabayashi, H. Shoji, S. Ogita, *Sumitomo Electric Industries, Yokohama, Kanagawa, Japan*

4:30 p.m.
E.3 **Silicon Photonic Modulator based on a MOS-Capacitor and a CMOS Driver (Invited)**
M. Webster, C. Appel, P. Gothoskar, S. Sunder, B. Dama, K. Shastri, *Cisco Systems, Allentown United States*

5:00 p.m.
E.4 **Gallium Arsenide Electro-Optic Modulators**
R. Walker[1], M. O'Keefe[1], N. Cameron[1], H. Ereifej[2], T. Brast[3], *[1]Finisar UK Ltd., Sedgefield, U.K., [2]Finisar Inc., Horsham, United States, [3]Finisar Germany GmbH, Berlin, Germany*

5:20 p.m.
End of Session E

Technology Exhibition
Opening Reception
Pavilion
6:00 p.m. - 7:30 p.m.

Tuesday, October 21st, 2014

REGISTRATION AND BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – Grand Foyer
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Pavilion

SESSION F: mm-Wave & THz Arrays

8:30 a.m. – 9:40 a.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: Shahriar Shahramian, *Bell Laboratories*
Kazuya Yamamoto, *Mitsubishi Electric*

8:30 a.m.
F.1 **Wafer-Scale Millimeter-Wave Phased-Array RFICs (Invited)**
G. Rebeiz, *UCSD, La Jolla, United States*

9:00 a.m.
F.2 **245 GHz SiGe Transmitter Array for Gas Spectroscopy**
K. Schmalz[1], J. Borngräber[1], W. Debski[2], M. Elkhouly[1], R. Wang[1], P. Neumaier[3], H. Hübers[3,4], *[1]IHP, Frankfurt (Oder), Germany, [2]Silicon Radar, Frankfurt (Oder), Germany, [3]Deutsches Zentrum für Luft- und Raumfahrt (DLR), Berlin, Germany, [4]Technische Universität Berlin, Berlin, Germany*

9:20 a.m.
F.3 **A Compact 340 GHz 2x4 Patch Array with Integrated Subharmonic Gilbert Core Mixer as a Building Block for Multi-Pixel Imaging Frontends**
Y. Karandikar, Y. Yan, V. Vassilev, H. Zirath, *Chalmers University of Technology, Gothenberg, Sweden*

9:40 a.m.
End of Session F

SESSION G: Emerging Technologies and Devices

8:30 a.m. – 10:00 a.m.
Aventine D,E – Hyatt Regency La Jolla at Aventine

Chairpersons: Paul Rosenthal, *Boeing*
Han Wui Then, *Intel Corp*

8:30 a.m.
G.1 **Diverse Accessible Heterogeneous Integration (DAHI) at Northrop Grumman Aerospace Systems (NGAS) (Invited)**
A. Gutierrez-Aitken, K. Hennig, D. Scott, K. Sato, W. Chan, B. Poust, X. Zeng, K. Thai, E. Nakamura, E. Kaneshiro, C. Monier, I. Smorchkova, B. Oyama, A. Oki, R. Kagiwada, G. Chao, *NGAS, Redondo Beach, United States*

9:00 a.m.
G.2 **Enabling Power-Efficient Designs with III-V Tunnel FETs (Invited)**
M. Kim, H. Liu, K. Swaminathan, X. Li, S. Datta, V. Narayanan, *Pennsylvania State University, University Park, United States*

9:30 a.m.
G.3 **Device Perspective on 2D Materials (Invited)**
P. Ye, *Purdue University, West Lafayette, United States*

Tuesday, October 21st, 2014

10:00 a.m.
End of Session G

10:00 a.m. - 10:30 a.m.
Coffee Break

PANEL SESSION 1: Will Silicon Photonics Rule the World of Optical Communications?

10:30 a.m. – 12:00 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Moderators: Thé Linh Nguyen, *Finisar Corporation*
Kumar Lakshmikumar, *Cisco Systems*

In this panel discussion industry experts will put forward their perspectives on the potential uses of Silicon Photonics and/or Compound-Semiconductor Photonics for various applications, such as high-performance computing, datacenter and long-haul transport, and very short-reach interconnects. Properties of the materials and devices give unique advantages to certain technologies in specific applications when parameters like power dissipation, form factor and cost are considered. Will the adage in the Compound-Semiconductor world - "If you want to compete with CMOS, don't"- hold true with Silicon Photonics?

Panel Members:

Adam Carter	*Cisco Systems*
Brian Welch	*Luxtera*
Sylvie Menezo	*LETI*
Daniel Mahgerefteh	*Finisar Corporation*
Naoya Kono	*Sumitomo Electric Industries*
Nobuhiro Kikuchi	*NTT Photonics Labs*
Andreas Umbach	*U^2T acquired by Finisar Corporation*

12:00 p.m.
End of Panel Session 1

12:00 p.m. – 1:30 p.m.
Break for Lunch

Technology Exhibition Lunch Pavilion
12:00 p.m. – 1:30 p.m.

Tuesday, October 21st, 2014

SESSION H: High-Speed Optical Communication Components

1:30 p.m. – 3:10 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: The'Linh Nguyen, *Finisar*
Yuriy Greshishchev, *Ciena Corporation*

1:30 p.m.
H.1 **Hybrid III-V Silicon Lasers: Heterogeneous 200mm-Wafer-Level Integration for WDM Dense Optical Interconnects (Invited)**
S. Menezo, H. Duprez, A. Descos, D. Bordel, L. Sanchez, P. Brianceau, V. Carron, B. Bakir, *CEA-Leti, Grenoble, France*

2:00 p.m.
H.2 **Optical Phase- Locking and Wavelength Synthesis (Invited)**
M.. Rodwell[1], H.C. Park[1], M. Piels[1], M. Lu[1], A. Sivananthan[1], E. Bloch[1], Z. Griffith[2], M. Urteaga[2], L. Johansson[1], J. Bowers[1], L. Coldren[1], [1]*University of California, Santa Barbara, United State.*[2], *Teledyne Scientific, Thousands Oak, United States*

2:30 p.m.
H.3 **InP DHBT Mux-Drivers for Very High Symbol Rate Optical Communications**
J. Godin, J. Dupuy, F. Jorge, F. Blache, M. Riet, V. Nodjiadjim, P. Berdaguer, B. Duval, A. Konczykowska, *III-V Lab, Joint Marcoussis, France*

2:50 p.m.
H.4 **A 25Gb/s Common Cathode VCSEL Driver**
K. Ng, Y. Choi, K. Wang, *Hong-Kong Applied Science and Technology Research Institute, Hong-Kong*

3:10 p.m.
End of Session H

SESSION I: High Efficiency Power Amplifier Architectures

1:30 p.m. – 3:00 p.m.
Aventine D,E – Hyatt Regency La Jolla at Aventine

Chairpersons: David W. Runton, *M/A-COM Tech. Solutions Inc.*
Rik Jos, *NXP Semiconductors*

1:30 p.m.
I.1 **Power Amplifier Design Optimized for Envelope Tracking (Invited)**
G. Collins, *MaXenctric Technologies, La Jolla, United States*

2:00 p.m.
I.2 **GaN Technology in Base Stations – Why and When?**
E. Higham, *Strategy Analytics, Newton, United States*

2:20 p.m.
I.3 **Development of High-Efficiency X-band Outphasing Transmitter**
C. Xie, D. Cripe, D. Landt, A. Walker, *Rockwell Collins, Cedar Rapids, United States*

Tuesday, October 21st, 2014

2:40 p.m.
I.4 **Broadband Doherty Alternative with Filter Design Considerations**
J. Jones, B. Noori, J. Frei, E. Krvavac, *Freescale Semiconductor, Tempe, United States*

3:00 p.m.
End of Session I

3:00 p.m. - 3:30 p.m.
Coffee Break

PANEL SESSION 2: Heterogeneous Integration – "Why is there III-V on my CMOS?"

3:30 p.m. – 5:00 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Moderators: Carl Dohrman, *Booz Allen Hamilton*
Paul Rosenthal, *Boeing*

The device-level combination of two or more dissimilar microelectronic technologies, or heterogeneous integration (HI) has increased circuit design flexibility, enabling electrical performance enhancements as compared to other advanced technologies such as SiGe BiCMOS. Some examples of HI technologies are InP HBTs integrated with deep-submicron Si CMOS, and GaN HEMTs with Si CMOS. However, the use of different material systems raises additional issues of thermal management, yield, cycle time, and reliability, to name just a few. Why go to the trouble of HI if circuit designers can achieve similar performance in SiGe BiCMOS? What are the specific performance boundaries outside of which one would choose to design in a HI technology? Is HI likely to emerge as a cost-effective solution for commercial applications, or is it destined to be reserved for performance-enhancing "niche" applications? What are the latest efforts to integrate efficient III-V optoelectronic components into a low cost Si platform?

Questions for the panel include:

• What are the best circuit applications for HI? Can these be achieved with SiGe BiCMOS? What are the expected market sizes for these applications?
• What are the thermal challenges created by HI?
• What wafer volume is required for acceptable yield in HI technologies?
• How does the reliability of each HI technology compare with SiGe BiCMOS?

Panel Members:

Thomas Kazior	*Raytheon*
Augusto Gutierrez-Aitken	*NGAS*
Tahir Hussain	*HRL*
Paul Franzon	*NC State University*
Dan Sparacin	*Aurrion*
Ed Preisler	*TowerJazz*

5:00 p.m.
End of Panel Session 2

Tuesday, October 21st, 2014

DHS SPECIAL PRESENTATION: Overview of the Chemical Facility Anti-Terrorism Standards Program

5:30 p.m. – 5:45 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Speaker: R. Locket, *Dept. of Homeland Security*

Chemicals are a vital component of modern life - from semiconductor fabrication to food processing - but the same chemicals that strengthen American industry, fertilize crops, fuel our vehicles, and assist in medical advances are also potentially attractive targets for those wishing to cause harm to the United States. Some chemical facilities possess materials that could be stolen or diverted and used as or converted into weapons, and a successful attack on certain high-risk facilities could potentially cause a significant number of deaths and injuries through the release of toxic substances or explosion. Responsibility for chemical security is shared among federal, state, and local governments, as well as the private sector. The Department of Homeland Security (DHS) has issued Chemical Facility Anti-Terrorism Standards (CFATS) for any facility that manufactures, uses, stores, or distributes certain chemicals at or above a specified quantity. Government and industry must work together to strengthen the security of America's chemical facilities, while not undercutting an important part of the nation's economy. In October 2006, Congress authorized DHS to regulate security at chemical facilities that DHS determines are high-risk. In order to do so, DHS created the CFATS program, which apply to any facility that manufactures, uses, stores, or distributes certain Chemical of Interest (COI) listed on the CFATS "Appendix A" at or above a specified quantity. CFATS is administered by the Infrastructure Security Compliance Division, part of the National Protection and Programs Directorate, Office of Infrastructure Protection. CFATS is a risk-based performance program that sets the standards for security at the Nation's highest risk chemical facilities. High-risk facilities contain COI that give rise to one or more security issues to include: release of toxic chemicals, theft or diversion of chemicals, and chemicals that can be used for sabotage or contamination. CFATS establishes Risk-Based Performance Standards (RBPS) for security issues such as perimeter security, access control, personnel surety, and cyber security, however not all high-risk facilities will need to take action to satisfy each RBPS. CFATS covered facilities are also required to have a Site Security Plan (SSP) that addresses RBPS. A facility's SSP will be tailored to its specific tier level, security issues, risks, and circumstances, as determined by DHS' review of its Security Vulnerability Assessment.

Tuesday, October 21st, 2014

PANEL SESSION 3: My IC doesn't work – whose fault is that?

5:45 p.m. – 7:15 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Moderators: Shuoqi Chen, *TriQuint Semiconductor*
Steve Huettner, *Nuvotronics LLC*

Despite increasingly sophisticated and powerful IC design tools and verified process design kits (PDKs), it's still a challenge for experienced designers to achieve first-pass success using the latest generation compound semi-conductor processes. This is particularly true for ICs that are designed for high frequency, output power, efficiency, and linearity in increasingly complex applications. Circuit designers ultimately must answer to management whether failures are due to one or a combination of device modeling, EM simulation, design methodology, mask layout, wafer processing, fixture/package assembly, and/or test technique. Trouble-shooting IC performance issues involves all aspects of process, modeling, design, and testing, and usually must be done quickly so that corrective action can be taken. This panel will discuss who (or what) might be responsible for design failure and how to increase the odds of achieving IC success at the first run. Our seasoned panelists will present their ideas and experiences to avoid mistakes and issues. Questions for the panel include:

• What type of circuit failures have often been observed at the first run?
• What are typically the least accurate elements in a PDK? Do you have better luck using measured S-parameters for some elements? Have you been burned by reference plane misunderstandings?
• Have you ever regretted *not* checking for standing waves at very high-power and burned off an open circuit stub in a matching network?
• Could better DRC or LVS have spotted the problem? Have you ever had an issue caused by translation between design and layout tools?
• Do time constraints play a part? Are answering to design review checklists a help or a hindrance?
• Have you ever been a victim of company politics? Are other organizations more than happy to see you fail?
• Does it pay to hedge your designs with features that can be removed at test? Have you had success in just changing the top metal layers of a mask set to correct a design?
• What is the best method of determining the minimal number of off-chip components in bias circuits to ensure stable operation?

A cash bar serving beer, wine, and soft drinks will be provided during this panel session.

Panel Members:

Chuck Campbell	*TriQuint Semiconductor*
Nick Cheng	*Skyworks Inc.*
James Komiak	*BAE Systems*
Chip Moyer	*HRL Laboratories*
Jim Schellenberg	*QuinStar Technology*

7:15 p.m.
End of Panel Session 3

Wednesday, October 22nd, 2014

REGISTRATION AND CONTINENTAL BREAKFAST

7:00 a.m. – 5:00 p.m.
Registration – Grand Foyer– Hyatt Regency La Jolla at Aventine
7:00 a.m. – 8:30 a.m.
Continental Breakfast – Foyer C

SESSION J: GaN Modeling

8:30 a.m. – 10:00 a.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: Faramarz Kharabi, *RFMD*
Kenneth K. Chu, *BAE Systems*

8:30 a.m.
J.1 **Status of the GaN HEMT Standardization Effort at the Compact Model Coalition (Invited)**
S. Mertens, *Agilent, EEsof EDA, Santa Clara, United States*

9:00 a.m.
J.2 **Symmetrical Modeling of GaN HEMTs**
A. Prasad[1], C. Fager[1], M. Thorsell[1], C. Andersson[3] K. Yhland[1,2], [1]*Chalmers University of Technology, Göteborg, Sweden*, [2]*SP Technical Research Institute of Sweden, Borås, Sweden*, [3]*Mitsubishi Electric Corporation, Kamakura, Japan*

9:20 a.m.
J.3 **First Pass Multi Cell Modeling Strategy for GaN Package Devices**
S. Halder, J. McMacken, J. Gering, *RFMD, Greensboro, United States*

9:40 a.m.
J.4 **Model Development for Monolithically-Integrated E/D-Mode Millimeter-Wave InAlN/AlN/GaN HEMTs**
J. Ren[1], B. Song[1], H. G. Xing[1], S. Chen[2], A. Ketterson[2], E. Beam[2], T. Chou[2], M. Pilla[2], H. Tserng[2], X. Gao[3], P. Saunier[2], P. Fay[1], [1]*University of Notre Dame, Notre Dame, United States*, [2]*TriQuint Semiconductor, Richardson, United States*, [3]*IQE RF, Somerset, United States*

10:00 a.m.
End of Session J

SESSION K: mm-Wave & THz Subsystems

8:30 a.m. – 10:10 a.m.
Aventine D,E – Hyatt Regency La Jolla at Aventine

Chairpersons: Frank E. van Vliet, *TNO*
Marc Rocchi, *OMMIC*

8:30 a.m.
K.1 **SiGe Transmitter and Receiver Circuits for Emerging Terahertz Applications (Invited)**
U. Pfeiffer[1], J. Grzyb[1], R. Al Hadi[1], N. Sarmah[1], K. Statnikov[1], S. Malz[1], B. Heinemann[2], [1]*University of Wuppertal, Wuppertal, Germany*, [2]*IHP GmbH, Frankfurt (Oder), Germany*

Wednesday, October 22nd, 2014

9:00 a.m.
K.2 **Silicon Wireless Systems for 60-GHz Consumer and Infrastructure Applications (Invited)**
A. Tomkins, A. Poon, E. Juntunen, A. El-Gabaly, G. Temkine, Y. To, C. Farnsworth, A. Tabibiazar, M. Fakharzadeh, S. Jafarlou, H. Tawfik, B. Lynch, M. Tazlauanu, R. Glibbery, *Peraso Technologies Inc., Toronto, Canada*

9:30 a.m.
K.3 **An Active Double-Balanced Down-Conversion Mixer in InP/Si BiCMOS Operating from 70-100 GHz**
J. McCue[1], M. Casto[1,2], J. C. Li[3], P. Watson[2], W. Khalil[1], *[1]The Ohio State University, Columbus, United States, [2]The Air Force Research Laboratory, Wright-Patterson AFB, United States, [3]HRL Laboratories, LLC, Malibu, United States*

9:50 a.m.
K.4 **GaN Technology for E, W, and G-band Applications**
A Margomenos[1], A. Kurdoghlian[1], M. Micovic[1], K. Shinohara[1], D. Brown[1], A. Corrion[1], H. Moyer[1], S. Burnham[1], D. Regan[1], R. Grabar[1], C. McGuire[1], M. Wetzel[1], R. Bowen[1], P. Chen[1], HTai[1], A. Schmitz[1], H. Fung[1], A. Fung[2], D. H. Chow[1], *[1]HRL Laboratories, LLC, Malibu , United States, [2]Jet Propulsion Laboratories, California Institute of Technology, Pasadena, United States*

10:10 a.m.
End of Session K

10:00 a.m. - 10:30 a.m.
Coffee Break

SESSION L: Evaluation and Modeling of High-Power and High-Speed Devices

10:30 a.m. – 11:50 a.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: Michael Schroter, *UCSD/TUD*
Rob Jones, *Raytheon*

10:30 a.m.
L.1 **An evaluation of extraction methods for the emitter resistance for InP DHBTs**
T. Nardmann[1], J. Krause[1], M. Schroter[2], *[1]TU Dresden, Dresden, Germany, [2]UC San Diego, La Jolla, United States*

10:50 a.m.
L.2 **The Impact of Electro-thermal Coupling on RF Power Amplifier Performance**
M. Ozalas, *Agilent Technologies, Santa Rosa, United States*

11:10 a.m.
L.3 **Analysis of the Influence of Layout and Technology Parameters on the Thermal Impedance of GaAs HBT/BiFET Using a Highly-Efficient Tool**
A. Magnani[1], V. d'Alessandro[1], L. Codecasa[2], P. Zampardi[3], B. Moser[3], N. Rinaldi[1], *[1]University of Naples, Naples, Italy, [2]Politecnico di Milano, Milano, Italy, [3]RFMD, Greensboro, United States*

11:30 a.m.

L.4 **Evaluation and Modeling of Voltage Stress-Induced Hot Carrier Effects in High-Speed SiGe HBTs**
G. Sasso[1], C. Maneux[2], J. Boeck[3], V. d'Alessandro[1], K. Aufinger[3], T. Zimmer[2], N. Rinaldi[1], *[1]University of Naples, Naples Frederico II, Naples, Italy, [2]IMS, University Bordeaux, Bordeaux, France, [3]Infineon Technologies AG, Neubiberg, Germany*

11:50 a.m.
End of Session L

SESSION M: High Frequency Power Amplifiers

10:30 a.m. – 11:50 a.m.
Aventine D,E – Hyatt Regency La Jolla at Aventine

Chairpersons: Simon Wood, *Cree*
Frank van Vliet, *TNO*

10:30 a.m.

M.1 **Miniaturization of Ka-band High Power Amplifier by 0.15 um GaN MMIC Technology**
K.S. Kong, M-Y Kao, A. Nayak, *TriQuint Semicondutor, Richardson, United States*

10:50 a.m.

M.2 **X-Ku wide-bandwidth GaN HEMT MMIC Amplifier with Small Deviaton of Output Power and PAE**
Y. Niida, Y. Kamada, T. Ohki, S. Ozaki, K, Makiyama, N. Okamoto, M. Sato, S. Masuda, K. Watanabe, *Fujitsu Laboratories, Atsugi, Kanagawa, Japan*

11:10 a.m.

M.3 **A 6-12 GHz Push-Pull GaN Amplifier for Low Harmonic Drive Applications**
M. Roberg, B. Kim, *TriQuint Semiconductors, Richardson, United States*

11:30 a.m.

M.4 **Investigation of various envelope complexity linearity under modulated stimulus using a new envelope formulation approach**
F. Ogboi[1], P. Tasker[1], M. Akmal[1], J. Lees[1], J. Benedikt[1], S. Bensmida[2], K. Morris[2], M. Beach[2], J. McGeehan[2], *[1]Cardiff University , Cardiff, United Kingdom, [2]University of Bristol, Bristol, United Kingdom*

11:50 a.m.
End of Session M

Wednesday, October 22nd, 2014

PANEL SESSION 4: Should Universities Continue to Teach Bipolar and III-V Technologies?

12:00 p.m. – 1:30 p.m.
Aventine A,B,C– Hyatt Regency La Jolla at Aventine

Moderators: Shahriar Shahramian, *Bell Laboratories*
Zachary Griffith, *Teledyne Scientific Company*

With the wide industry adoption of CMOS technology as the process of choice for a variety of applications, universities often opt to eliminate or limit the teaching of bipolar and III-V technologies from their curriculum. This in turn may shape the course of technology adoption in the future as compound semiconductor expertise dwindles. Furthermore, heavy reliance on computer aided design methodology may inadvertently lead to a lack fundamental and theoretical understanding of circuit design techniques. Multi-core and distributed simulation capabilities allow designers to execute multidimensional optimization routines to arrive at the desired circuit components parameters without ever needing to perform theoretical analysis.

This panel discusses the pros and cons of a CMOS-centric education system as well as views on theoretical design methodology versus computer-aided optimization techniques. Should universities only teach CMOS circuit design? How can educators take advantage of computer aided design approaches without diluting the classic intuitive and theoretical design approaches?

Panel Members:

Gabriel Rebeiz	*University of California San Diego*
Mark Rodwell	*University of California Santa Barbara*
Jon Hacker	*Teledyne Scientific Company, LLC*
Sorin Voinigescu	*University of Toronto*

Given the time of this panel, the hotel store “Perks” in the lobby has been heavily stocked with sandwiches, snacks, and beverages to quickly grab before the session.

1:30 p.m.
End of Panel Session 4

SESSION N: Applications of Next Generation Technologies

1:30 p.m. – 3:00 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: Steve Huettner, *Nuvotronics LLC*
Jim Carroll, *NI-AWR Group*

1:30 p.m.
N.1 **W-band GaN Receiver Components Utilizing Highly Scaled, Next Generation GaN Device Technology (Invited)**
A Margomenos, A. Kurdoghlian, M. Micovic, K. Shinohara, H. Moyer, D. C. Regan, R. M. Grabar, C. McGuire, M. Wetzel, D. Chow, *HRL Laboratories, LLC, Malibu, United States*

2:00 p.m.
N.2 **Ka band chip-set for Electronically Steerable Antennas**
R. Leblanc, N. Ibeas, A. Gasmi, J. Moron
OMMIC SAS, Limeil Brévannes, France

Wednesday, October 22nd, 2014

2:20 p.m.
N.3 **12.5 THz Fco GeTe Inline Phase-Change Switch (IPCS) Technology for Reconfigurable RF and Switching Applications**
N. El-Hinnawy, P. Borodulin, E. Jones, B. Wagner, M. King, J. Mason Jr., J. Paramesh, J. Bain, R. Howell, M. Lee, R. Young, *Northrop Grumman Electronic Systems, Linthicum, United States*

2:40 p.m.
N.4 **Low Loss, High Performance 1-18 GHz SPDT Based on the Novel Super-Lattice Castellated Field Effect Transistor (SLCFET)**
R. Howell, E. Stewart, R. Freitag, J. Parke, B. Nechay, H. Cramer, M. King, S. Gupta, J. Hartman, P. Borodulin, M. Snook, I. Wathuthanthri, P. Ralston, K. Renaldo, G. Henry, *Northrop Grumman Electronic Systems, Linthicum, United States*

3:00 p.m.
End of Session N

SESSION O: Mixed Signal Circuits

1.30 p.m.- 2.30 p.m.
Aventine D,E – Hyatt Regency La Jolla at Aventine

Chairpersons: James Buckwalter, *UC San Diego*
Hui Pan, *Broadcom, Irvine*

1.30 p.m.
O.1 **1700 pixels per inch (PPI) Passive-Matrix Micro-LED Display Powered by ASIC**
W. Chong[1], W. Cho[1], Z. Liu[1], C. Wang[2], K. Lau[1], *[1]Hong Kong University of Science and Technology, Hong Kong, [2]3C Limited, Hong Kong*

1:50 p.m.
O.2 **Programmable Active Clock Spine for 100Gb/200Gb Coherent Optical Receiver Chip in 32nm CMOS**
N. Ben-Hamida, C. Kurowski, R. Gibbins, J. Weng, T. Wong, J. Lindsay, H. Mah, S. Aouini, A. McCarthy, *Ciena Corp., Ottawa, Canada*

2:10 p.m.
O.3 **A 7-8 GHz Serrodyne Modulator in SiGe for MIMO Signal Generation**
J. Withagen[1], A. Annema[1], B. Nauta[1], F. van Vliet[2], *[1]University of Twente, Enschede, The Netherlands, [2]TNO, The Hague, The Netherlands*

2:30 p.m.
End of Session O

Wednesday, October 22nd, 2014

SESSION P: Breaking News Papers

3:30 p.m. – 5:05 p.m.
Aventine A,B,C – Hyatt Regency La Jolla at Aventine

Chairpersons: Douglas S. McPherson, *Ciena*
Charles F. Campbell, *TriQuint Semiconductor*

3:30 p.m.
Student Paper Competition Winner Pronouncement

3:35 p.m.
P.1 **A Highly Integrated Chipset for 40 Gbps Wireless D-band Communication Based on a 250 nm InP DHBT Technology**
S. Carpenter[1], Z. He[1], M. Bao[2], H. Zirath[1,2], *[1]Microwave Electronics Laboratory, Department of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden, [2]Ericsson Research, Ericsson AB, Göteborg, Sweden*

3:50 p.m.
P.2 **Characterization of the High Frequency Performance of 28-nm FDSOI MOSFETs as a Function of Backgate Bias**
S. Shopov, S. Voinigescu, *University of Toronto, Toronto, Canada*

4:05 p.m.
P.3 **An 8-bit 140-GHz Power-DAC Cell for IQ Transmitter Arrays with Antenna Segmentation**
S. Shopov, S. Voinigescu, *University of Toronto, Toronto, Canada*

4:20 p.m.
P.4 **Advanced Process and Modeling on 600+ GHz Emitter-Ledge Type-II GaAsSb/InP DHBT**
H. Xu[1], B. Wu[2], A. Winoto[1], M. Feng[1], *[1]University of Illinois at Urbana-Champaign, Urbana, United States, [2]High Frequency Technology Center, Agilent Technologies, Inc., Santa Rosa, United States*

4:35 p.m.
P.5 **170 GHz SiGe-BiCMOS Loss-Compensated Distributed Amplifier**
P. Testa, G. Belfiore, C. Carta, F. Ellinger, *Technische Universität Dresden, Dresden, Germany*

4:50 p.m.
P.6 **Direct Down-conversion 38 GHz GaAs and SiGe Receivers**
R. Clement[1,3], L. Milner[2], E. Convert[1], L. Hall[2], M. Parker[2], M. McCulloch[1], A. Dadello[1], B. Wu[1], J. Harvey[1], A. Parker[1,3], Simon J. Mahon[1], *[1]MA-COM, North Sydney, Australia, [2]Defence Science and Technology Organization, Edinburgh, Australia, [3]Macquarie University, New South Wales, Australia*

5:05 p.m.
End of Session P

Close of Symposium

2014 IEEE CSIC Symposium Organizers

EXECUTIVE COMMITTEE

Douglas S. McPherson
Symposium General Chair
Ciena Corporation
Ottawa, ON, Canada

Charles Campbell
Technical Program Chair
TriQuint Semiconductor
Richardson, TX

Harris Moyer
Technical Program Vice Chair
HRL Laboratories, LLC
Malibu, CA

Jim Carroll
Local Arrangements Chair
NI-AWR GROUP
Dallas, TX

Douglas S. McPherson
Symposium Treasurer
Ciena Corporation
Ottawa, ON, Canada

Brian Moser
Symposium Publicity Chair
RFMD
Greensboro, NC

Peter Zampardi
Exhibit Chair
RFMD
Westlake Village, CA

Bruce Green
Publications Chair
Freescale Semiconductor
Tempe, AZ

Francois Colomb
Chair, Emeritus
Raytheon
Andover, MA

David Osika
Webmaster
Anadigics, Inc.
Warren, NJ

OVERSEAS ADVISORS

Marc Rocchi
OMMIC
Limeil Brevannes, France

Kazuya Yamamoto
Mitsubishi Electric Corporation
Hyogo, Japan

Tomoya Kaneko
NEC
Kawasaki, Japan

TECHNICAL PROGRAM COMMITTEE

Avram Bar-Cohen	**University of Maryland/DARPA-MT0**
James Buckwalter	**University of California San Diego**
Charles Campbell	**TriQuint Semiconductor**
Jim Carroll	**NI-AWR GROUP**
Shuoqi Chen	**TriQuint Semiconductor**
Myung-Jun Choe	**Teledyne Scientific Company**
Kenneth Chu	**BAE Systems**
Gilberto De la Rosa	**Anadigics Incorporated**
Bruce Green	**Freescale Semiconductor**
Yuriy Greshishchev	**Ciena Corporation**
Zachary Griffith	**Teledyne Scientific Company**
Hossein Hashemi	**University of Southern California**
Steve Huettner	**Nuvotronics LLC**
Kazutaka Inoue	**Sumitomo**
Rob Jones	**Raytheon Company**
Rik Jos	**NXP Semiconductors**
Tomoya Kaneko	**NEC Corporation**
Hooman Kazemi	**Nuvotronics LLC**
Waleed Khalil	**The Ohio State University**
Faramarz Kharabi	**RFMD**
Donald Kimball	**MaXentric Technologies**
Kazuaki Kunihiro	**NEC Corporation**
Kumar Lakshmikumar	**Cisco Systems**
Simon Mahon	**MA/Com Technology Solutions**
Joseph Maurer	**Booz Allen Hamilton**
Douglas McPherson	**Ciena**
Brian Moser	**RFMD**
Harris Moyer	**HRL Laboratories**
Munehiko Nagatani	**NTT Corporation**
Arun Natarajan	**Oregon State University**
Thé Linh Nguyen	**Finisar Corporation**
Sean Nicolson	**Broadcom**
Marc Rocchi	**OMMIC**
Mark Rodwell	**University of California at Santa Barbara**
Paul Rosenthal	**Boeing Satellite Development Center**
Dave Runton	**Nitronex LLC**
Michael Schroeter	**University of California San Diego**
Shahriar Shahramian	**Alcatel-Lucent**
Craig Steinbeiser	**TriQuint Semiconductor**
Paul Tasker	**Cardiff University**
Han Wui Then	**Intel Corporation**
Frank Traut	**Hittite Microwave Corporation**
Frank van Vliet	**TNO**
Noriyuki Watanabe	**NTT Photonics Labs**
Simon Wood	**Cree Incorporated**
Barry Wu	**Agilent Technologies**
Kazuya Yamamoto	**Mitsubishi Electric Corporation**
Peter Zampardi	**RFMD**
Qi Zhang	**Hittite Microwave Corporation**

IEEE ADVISORS

Shana Ramandi
IEEE Meeting & Conference Management
Piscataway, NJ
s.ramandi@ieee.org

Sherry Russ Sills
Director, Event Management Services
IEEE Meeting & Conference Management
Piscataway, NJ
s.russ@ieee.org

Jean Bae
EDS Conference Administrator
IEEE Electron Devices Society
Piscataway, NJ
jean.bae@ieee.org

Chris Jannuzzi
EDS Exective Director
IEEE Electron Devices Society
Piscataway, NJ
c.jannuzzi@ieee.org

CONFERENCE MANAGEMENT

Shana Ramandi
IEEE Meeting & Conference Management
445 Hoes Lane, Piscataway, NJ 08854 USA
Phone: + 1-732-465-5809
Email: s.ramandi@ieee.org

EXHIBIT MANAGEMENT

Candi Wooldridge
Exhibit Coordinator
MP Associates, Inc.
1721 Box Elder St., Ste. 107
Louisville, CO, 80027, USA
Tel: (310) 530-4562
FAX: (310) 530-4334
Email: candi@mpassociates.com

Susie Horn
Director of Exhibits Operations
MP Associates, Inc.
1721 Box Elder St., Ste. 107
Louisville, CO, 80027, USA
Tel: (310) 530-4562
FAX: (310) 530-4334
Email: susie@mpassociates.com

SYMPOSIUM HEADQUARTERS

Hyatt Regency La Jolla at Aventine
3777 La Jolla Village Drive,
San Diego, California, USA 92122
Tel: +1 858 552 1234
Fax: +1 858 552 6066
Web Site: http://www.hyattregencylajolla.com

SYMPOSIUM CHECKLIST

HOTEL RESERVATIONS

Click on the "Hotel" link on the conference website or go directly to:

https://resweb.passkey.com/Resweb.do?mode=welcome_ei_new&eventID=7392428

SYMPOSIUM REGISTRATION

Click on the "Online Registration" link on the www.csics.org conference website or go directly to:

http://www.cvent.com/d/lcqb0g

Or, click on the "Registration Form" link and mail, fax, or email the completed Registration Form to:

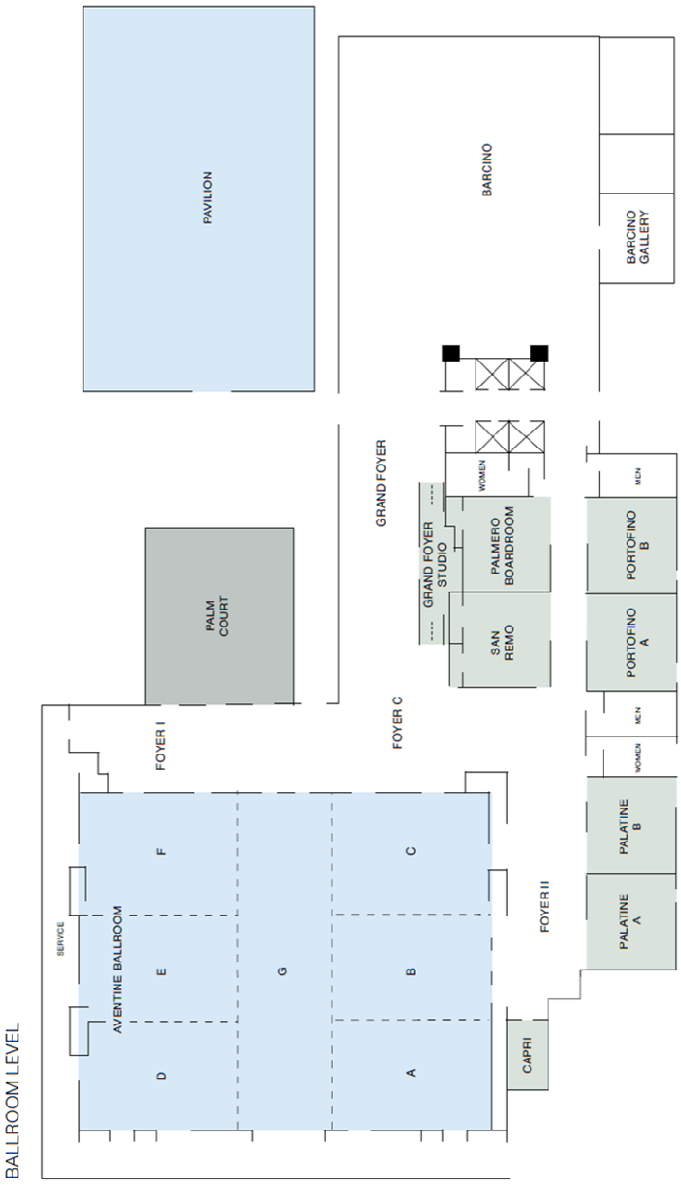
IEEE/MCM: Shana Ramandi
CSICS Registrar
445 Hoes Lane, Piscataway, New Jersey 08855 USA
Tel: +1-732-465-5809
Toll Free (US and Canada) +1-800-810-4333
FAX : +1-732-465-6447
Email: csicsreg@ieee.org

Advance registration deadline: September 26th.

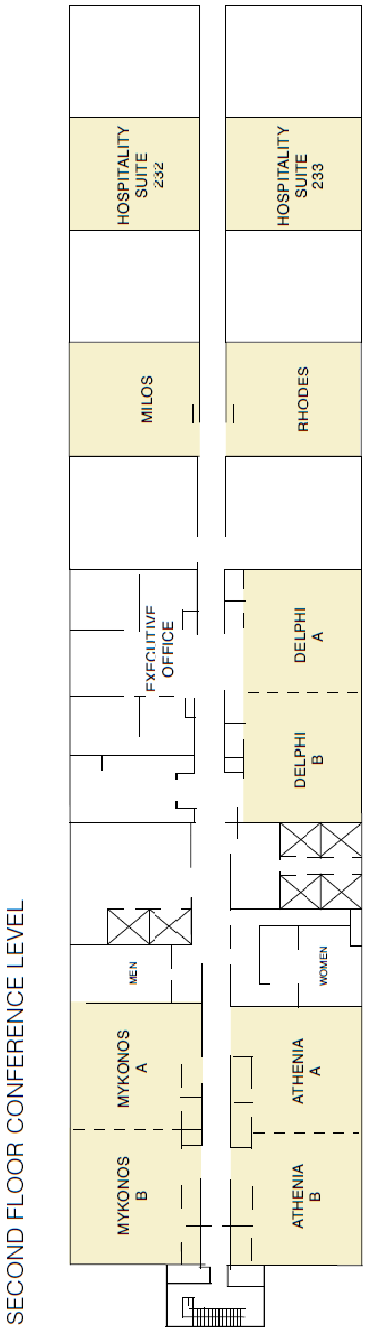
EXHIBITOR INFORMATION

Contact: **Candi Wooldridge**
Exhibit Coordinator
MP Associates, Inc.
1721 Box Elder St., Ste. 107
Louisville, CO, 80027, USA
Tel: (310) 530-4562
FAX: (310) 530-4334
Email: candi@mpassociates.com

Hyatt Regency La Jolla at Aventine
Floor 1

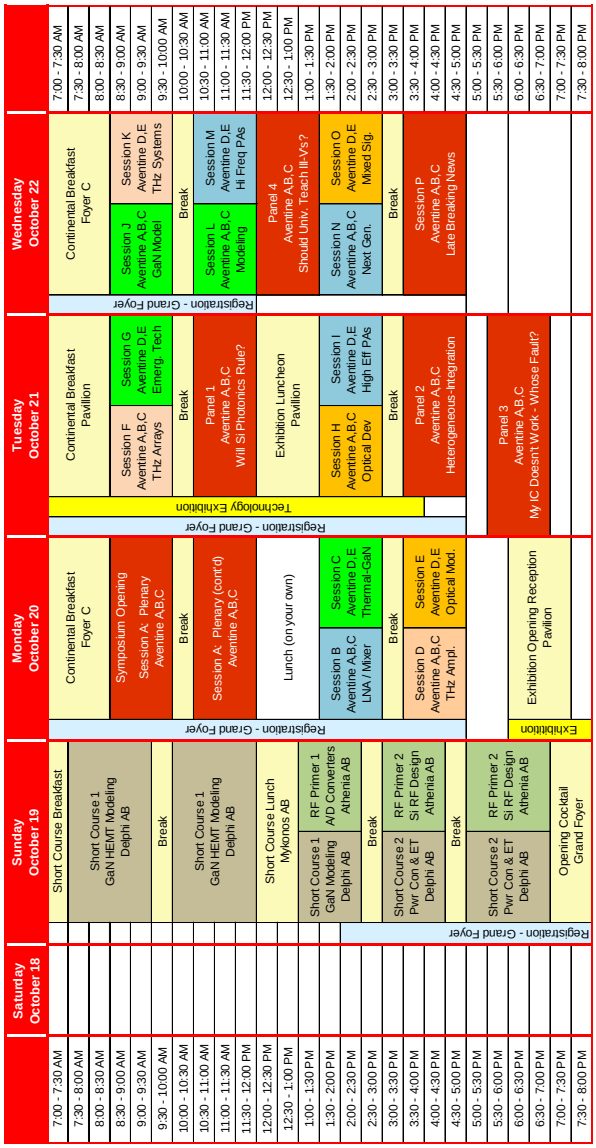


Hyatt Regency La Jolla at Aventine
Floor 2



CSICS Week – Schedule Overview

Please note that the times are approximate. Please refer to the detailed schedule on pp. 2 and 3



NOTES