Speakers' Corner

A Brief History of GaAs Technology at the GaAs IC Symposium and a Look Ahead to the 2015 CSICS

■ Bruce Green and Chuck Weitzel

Over the last four decades, the IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS), formerly the Gallium Arsenide Integrated Circuit (GaAs IC) Symposium, has brought III–V device and microwave circuit engineers and researchers together in a stimulating, highly engaging environment. This column provides some background on the symposium, as shown in the timeline history of Figure 1. It recounts the early history of GaAs technology advancements reported at the symposium and introduces the 2015 CSICS to be held in New Orleans, Louisiana, 11–14 October.

In the mid-1970s, GaAs RF technology was based on microwave ICs (MICs). These were not ICs in the sense that we know them today because they consisted of discrete active and passive components assembled on ceramic substrates. Commercial GaAs chips were manufactured by the large electronic Japanese conglomerates and a handful of small U.S. companies. At the time, a few forward-thinking R&D teams in the United States were pursuing GaAs digital ICs through government contracts. The GaAs IC Symposium was initiated to provide a public forum for this new digital IC technology based on GaAs. Some of these early pioneers were convinced that, in time, GaAs ICs would displace silicon (Si) ICs and become the workhorse of digital technology.

The first GaAs IC Symposium was held in 1979 in Lake Tahoe, California, with between 100 and 200 attendees. In the early years, the symposium digest was more like a pamphlet with single-page abstracts for each paper. The technical committee reviewed all submitted papers, but the acceptance criteria were very loose. Once, a very well-respected committee member proposed that any paper showing a reasonable device I–V characteristic on a curve tracer be accepted so that the technical community could hear how the device was fabricated. The symposium developed the reputation as the place to report the latest GaAs IC developments.

A Journey Through GaAs History at the GaAs IC Symposium

Virtually all the early advances in GaAs technology were reported at this symposium, and many advancements were needed. At this time, GaAs wafers were not round but rather D-shaped because the ingots were grown in a horizontal boat. If you needed to check something about how the device fabrication was proceeding, you did not hesitate to break off a small piece of the wafer for analysis. The brittleness of GaAs made this very easy. Following is a review of some early advances in GaAs technology.

Charles Evans provided the first insight into why some wafers did not retain their semi-insulating property during annealing.

A truly digital technology could not depend on the reproducibility and uniformity of epitaxial growth; therefore, an ion implantation technology was needed. This was a major issue because, when heated, GaAs starts outgassing arsenic at about 400 °C. This was clearly evident by the arsenic oxides (white powder) seen at the exhaust port of ohmic contact annealing furnaces. Therefore, a cap that would stand up to the ion implantation anneal temperature was needed. In the beginning, each R&D group had its own cap recipe that

Bruce Green (Bruce_Green@ieee.org) is the CSICS 2015 publicity chair.
Chuck Weitzel (c.weitzel@ieee.org) is a past GaAs IC TPC member and the 2015 IMS TPC chair.

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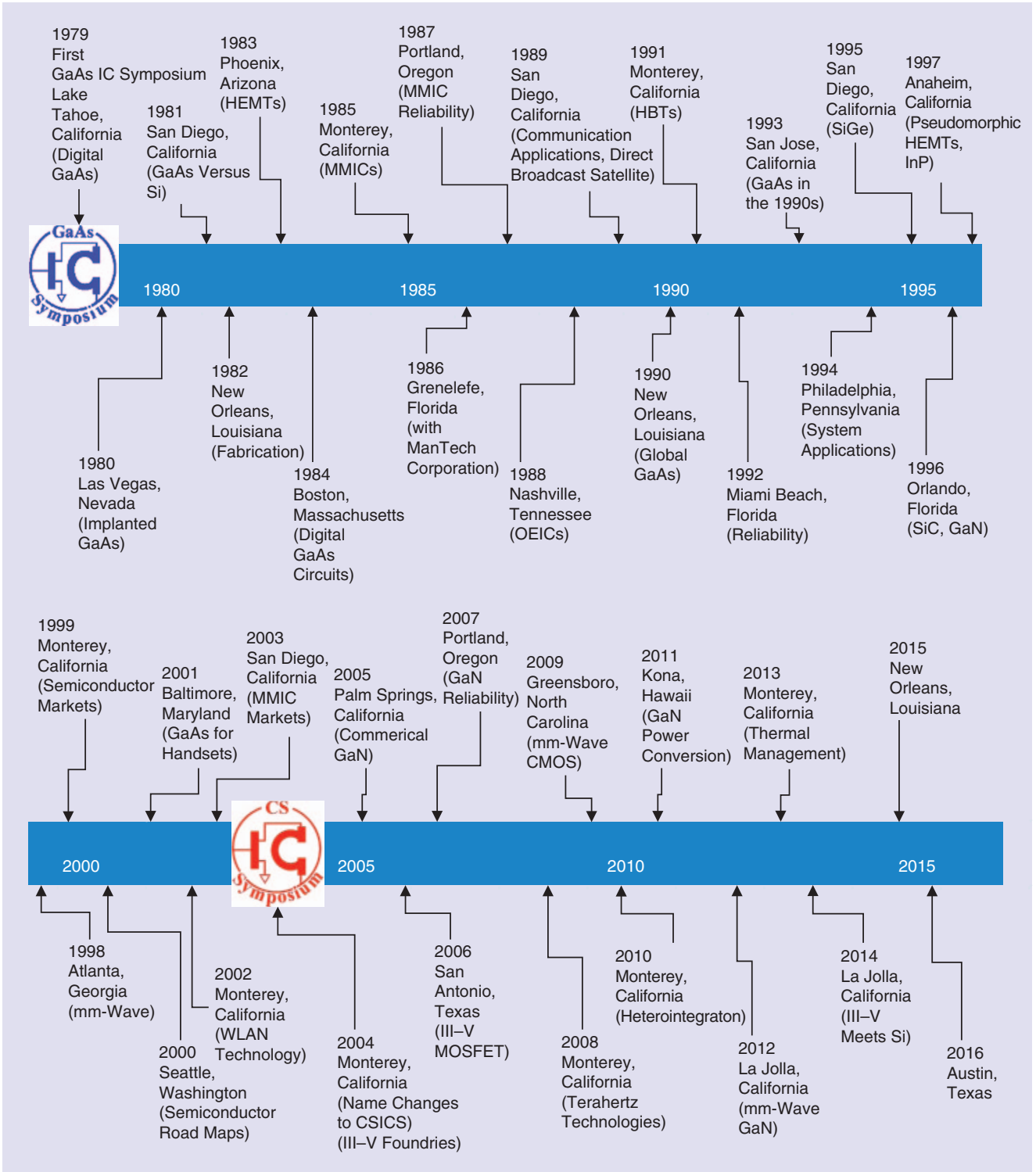

Figure 1. *A history of the GaAs IC Symposium and the CSICS at a glance, with "hot topics" in parentheses. Now in its 37th year, CSICS will continue its legacy of cutting-edge III–V technology in New Orleans in October 2015.*

included a wafer cleaning process and the deposition of a silicon nitride and/or silicon oxide cap.

Even if you had a cap that would not delaminate during annealing, some semi-insulating GaAs wafers could lose their semi-insulating property during annealing. This semi-insulating property significantly reduced substrate capacitance and, therefore, was essential for the high speed of GaAs digital ICs. At the time, semi-insulating GaAs wafers were doped with chromium (Cr) to create deep levels that trapped electrons, giving them this important property. After GaAs ingots were grown, crystal growers would supply sample wafers to potential buyers who would then try to qualify the Cr-doped substrate with their own proprietary capping process. If the sample wafer passed, the customers

would then purchase the other wafers from the same ingot in hopes that all the remaining wafers would work in their IC process. If a customer rejected a particular ingot, the wafer supplier would not hesitate to send a sample wafer from that same ingot to other customers in hopes that the ingot could be qualified in a different anneal process. This was the accepted practice at the time.

Charles Evans provided the first insight into why some wafers did not retain their semi-insulating property during annealing. The intentionally doped Cr was being depleted from the wafer surface during annealing even though the implant cap remained intact. GaAs wafers had to remain semi-insulating following the cap-and-anneal process to be suitable for digital ICs. At some point, boat-grown D-shaped GaAs wafers were replaced by round wafers grown by other processes, and other means were found to produce semi-insulating substrates without Cr doping.

The semi-insulating property of GaAs was not sufficient to perfectly isolate one digital device from a neighboring device.

Because the GaAs ohmic metal stack was gold based, all of the other metallization was also gold based. This required that the metal layers be formed using liftoff. At times, this process was very problematic and did not work as planned. Soaking the wafer in acetone for hours just did not help. One solution was to soak the exposed photoresist in chlorobenzene, which hardened the top layer. This produced an opening in the resist with a retrograde profile, making the liftoff process more reproducible, and increased device yield. This process was reported at the symposium.

Marty Lepselter was a well-respected Bell Labs researcher who, among other things, pioneered electron-beam lithography. He was quoted in a news release saying that short-gate-length Si would "blow GaAs out of the water." This comment led to a debate at the 1981 GaAs IC Symposium in San Diego. Marty's hypothesis was that short-gate-length Si digital ICs would outperform GaAs ICs, overcoming GaAs' higher electron mobility and low-capacitance semi-insulating substrate. Of course, each side believed that it had won the debate, but as we have seen, Marty was right about short-gate-length Si. The advent of the stepper pushed electron-beam lithography aside because of its higher wafer throughput.

Back gating was another phenomena reported at the symposium. The semi-insulating property of GaAs was not sufficient to perfectly isolate one digital device from a neighboring device. An isolated nearby ohmic contact could act as a parasitic gate electrode through the substrate. This could be seen on a curve tracer by connecting the parasitic gate pad to the gate electrode of the curve tracer. The saturated drain current could be modulated, and a small transconductance could be measured.

In addition to the technology problems that had to be solved, the GaAs digital gate that used depletion-mode field-effect transistors (FETs) had the added problem of needing to have an output-level shifting device. This meant that a GaAs digital gate required more devices than the equivalent digital gate in Si metal–oxide–semiconductor field-effect transistor (MOSFET) technology. These extra devices in the gate impeded the drive to higher-density GaAs ICs.

In the early 1980s, Fujitsu announced the first aluminum (Al) GaAs/GaAs heterojunction transistor. It is interesting that Bell Labs invented the heterojunction concept, but Fujitsu was the first to report a functioning device. These early heterojunction FETs would often have drifting dc characteristics as seen on a curve tracer. However, as we know, this problem was also solved and, along with many others, was reported at the GaAs IC Symposium. The success of these advancements was often demonstrated in terms of ring oscillators. When asked about the yield of his ring oscillators, the researcher would respond that his circuit yield was sufficient to meet the worldwide demand for ring oscillators.

Attendance at the GaAs IC Symposium swelled to more than 900 attendees in the mid-1980s as U.S. government funding floodgates for GaAs monolithic MIC (MMIC) technology opened, and many researchers rushed into the GaAs IC arena. It was also during this time that the advances in device technology discussed previously led to state-of-the-art GaAs MMICs. Also, new III–V technologies, such as indium phosphide (InP)-based high-electron-mobility transistor (HEMT) devices, began to mature and show state-of-the-art performance.

During the early and mid-1990s, researchers began to present papers on new technologies such as GaAs heterojunction bipolar transistors (HBTs) and silicon carbide (SiC) and gallium nitride (GaN) widebandgap semiconductors at the GaAs IC Symposium. As with GaAs device technology, these new devices had similar issues that had to be solved. The late 1990s also saw the rise of silicon-germanium (SiGe) HBT technology. At the same time, as GaAs HEMT and metal–semiconductor FET technologies matured, high-volume applications such as handset power amplifiers (PAs) became frequent topics at the GaAs IC Symposium. Like the debates over whether Si or GaAs would dominate high-speed digital devices more than a decade earlier, debates over whether SiGe HBTs or GaAs technology would dominate microwave PA applications figured prominently at the GaAs IC Symposium from 1998 to 2000.

During the early 2000s, new high-speed technologies, such as GaN, InP, and SiGe, became more mainstream and more frequent topics at the symposium. To reflect this, in 2004 the symposium's name was changed from the GaAs IC Symposium to the CSICS. With its new name, the CSICS has continued the GaAs IC Symposium legacy of top-quality papers in a congenial atmosphere.

The 2015 CSICS Carries on the Tradition of Cutting-Edge III–V Technology and Applications

Today, the CSICS covers state-of-the-art microwave/millimeter-wave (mm-wave) devices, ICs, and PAs in GaAs, GaN, InP, SiGe, and CMOS technologies.

Now in its 37th year, the CSICS has remained a premier symposium at which to present state-of-the-art results for both device and circuit technology. State-of-the-art device technology has included ultrahigh-speed as well as ultrahigh-power applications. Over the years, the GaAs IC Symposium and CSCIS have hosted papers on state-of-the-art MMIC PA power and efficiency, sample and hold circuit speed, mm-wave IC power, gigabit IC performance, frequency divider operating frequency, and many other state-of-the-art benchmarks. The symposium also showcases the latest advances in modeling and manufacturing technology. At the same time, the symposium has maintained its reputation for excellent short courses, primers, and panel sessions.

The 2015 CSICS at the Sheraton Hotel in New Orleans (see Figures 2 and 3) includes a three-day, dual-track technical program, two short courses, a primer course, and a technology exhibition. Also, for the second year, the CSICS will offer a student paper competition. The technical program includes 60–70 high-quality papers and four topical panel sessions.

This year, the CSICS is proud to announce over 20 internationally renowned invited speakers, notably Bruce Wallace (Defense Advanced Research Projects Agency), Zoya Popovic (University of Colorado, Boulder), John Volakis (Ohio State University), Ken Brown (Raytheon), Patrick Courtney (Qorvo), Bill Deal (Northrop Grumman), Kazuhiko Honjo (The University of Electrocommunications, Japan), Shogo Yamanaka (NEC), Takayuki Shibasaki (Fujitsu), Pascal Chevalier (ST Microelectronics), Jesus del Alamo (MIT), Eric Lind (Lund University), Ken Chu (BAE Systems), Akira Nakajima (National Institute of Advanced Industrial Science and Technology), Masataka Higashiwaki (National Institute of Information and Communications Technology), Thomas Zimmer (University of Bordeaux), Ian Betty (Ciena), Sam Palermo (Texas A&M), Noman Wolf (Heinrich Hertz Institute), Michel Poulin (TeraXion), and Efthymios Rouvalis (Finisar). These distinguished speakers will present the latest advances in SiGe bipolar CMOS, InGaAs MOSFETs, nanowire FET devices, enhancement-mode GaN HEMTs, device modeling, mm-wave/terahertz PAs and systems, spatially combined PAs, envelope-tracking PAs, and low-power receiver and transmitter circuits and digital signal processors, as well as Si and InP modulators and drivers.

Figure 2. *The Sheraton Hotel on Canal Street in New Orleans, the site of the 2015 CSICS. (Photo courtesy of Sheraton Hotels.)*

Figure 3. *Historic Jackson Square, New Orleans, a brief walk from the Sheraton Hotel. (Photo courtesy of Sheraton Hotels.)*

GaAs RF technology was based on microwave integrated circuits.

This year, the CSICS offers two in-depth short courses on Sunday, 11 October. The first, "Transmit and Receive IC Design for Fiber Optic Links," will be presented by leading experts The' Linh Nguyen (Finisair), Kumar Lakshmikumar (Cisco), and Mark Webster (Cisco). This course details high-speed analog IC design basics for electronic and optoelectronic applications. It will prove invaluable for anyone involved in high-speed electronic or optoelectronic devices, circuit design, or systems.

The second course, "Microwave Package Design Fundamentals," will be taught by leading high-speed packaging experts, including Tom Green (T.J. Green Associates). This course will cover the basics of microwave packaging for high-speed and high-power microwave applications. It will cover the packaging materials and technologies, assembly techniques, and design considerations for packaging high-frequency microwave and mm-wave devices. The course will be useful for device, circuit, and system designers.

On Sunday evening, Waleed Khalil (Ohio State University) will teach an expanded primer course on Si RFIC design. This three-and-a-half hour lecture is intended for participants of all technical backgrounds who wish to learn, or refresh their understanding of, the fundamentals of designing the principal circuit building blocks in radio and radar system on a chip. Among the blocks covered are PAs, low-noise amplifiers, mixers, voltage control oscillators, and integrated passives, with examples drawn from both CMOS and SiGe technology. The primer is an excellent way to start the symposium and is guaranteed to enhance attendee appreciation of the technical program.

In recognition of the exceptional contributions made by students, the CSICS is proud to hold its second Student Paper Competition. To participate in the competition, eligible students must submit a regular contributed paper naming, at a minimum, themselves and their principal supervisor as authors. The finalists must present their own papers at their assigned symposium session.

For registration and up-to-date information, please visit the CSICS Web site at www.csics.org. Further questions may be addressed to the symposium chair: Dr. Charles F. Campbell, tel.: +1 972 994 3644, e-mail: Charles.Campbell@qorvo.com.

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